## 256 MBit Synchronous DRAM

- High Performance:

| | -7.5 | -8 | -8A | Units |
|---|---|---|---|---|
| fCK | 133 | 125 | 125 | MHz |
| tCK3 | 7.5 | 8 | 8 | ns |
| tAC3 | 5.4 | 6 | 6 | ns |
| tCK2 | 10 | 10 | 12 | ns |
| tAC2 | 6 | 6 | 6 | ns |

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{\text{CAS}}$ Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8
- Full page burst length (optional) for sequential wrap around
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7,8 µs)
- Random Column Address every CLK ( 1-N Rule)
- Single 3.3V +/- 0.3V Power Supply
- LVTTL Interface versions
- Plastic Packages: P-TSOPII-54 400mil width (x4, x8, x16)
- -7.5 parts for PC133 3-3-3 operation
  -8 parts for PC100 2-2-2 operation
  -8A parts for PC100 3-2-2 operation

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The HYB39S256400/800/160CT(L) are four bank Synchronous DRAM's organized as 4 banks x 16MBit x4, 4 banks x 8MBit x8 and 4 banks x 4Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for $\overline{\text{CAS}}$-latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with INFINEON's advanced 0.17 µm 256MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

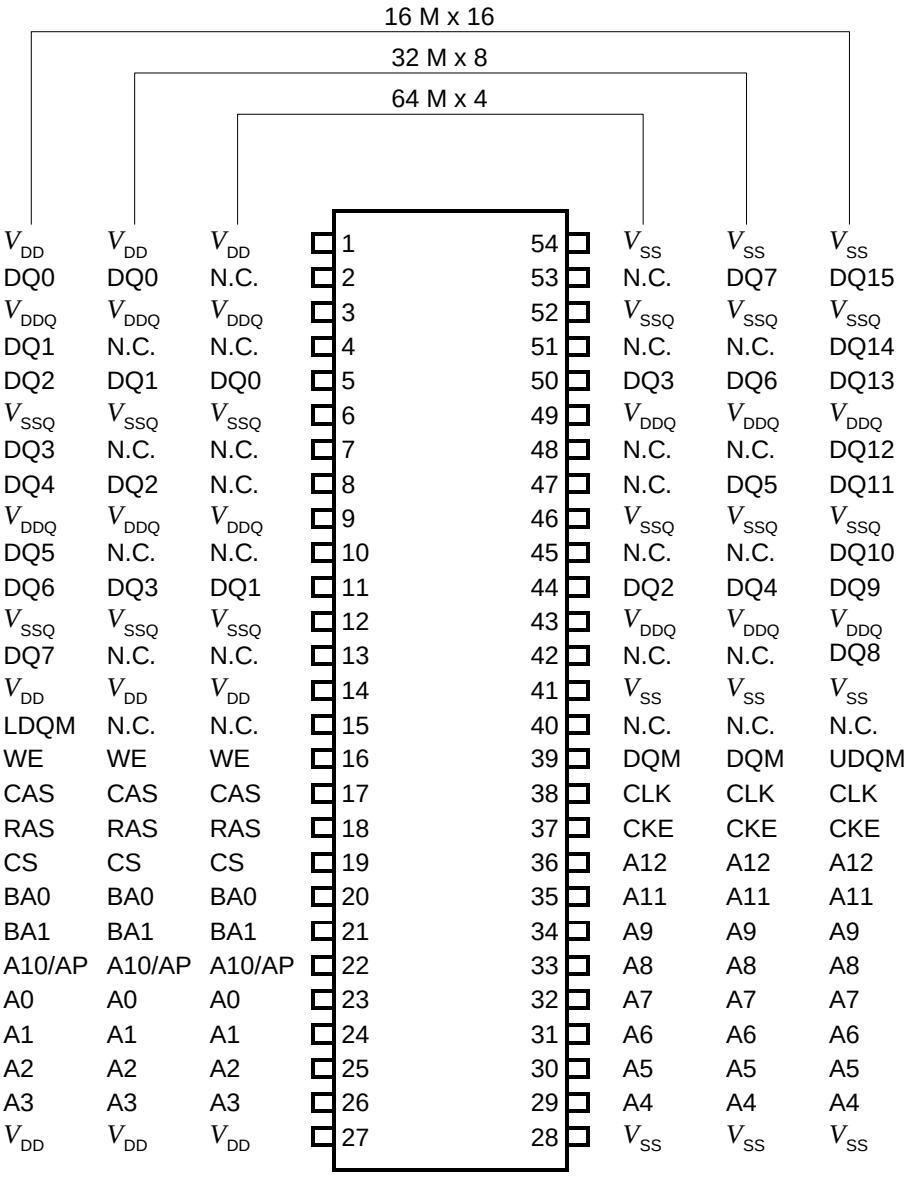
Auto Refresh (CBR) and Self Refresh operation are supported. These devices operates with a single 3.3V +/- 0.3V power supply and are available in TSOPII packages.

## Ordering Information

| Type | Speed Grade | Package | Description |
|---|---|---|---|
| | | | |
| HYB 39S256400CT-7.5 | PC133-333-520 | P-TSOP-54-2 (400mil) | 133MHz 4B x 16M x 4 SDRAM |
| HYB 39S256400CT-8 | PC100-222-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 16M x 4 SDRAM |
| HYB 39S256400CT-8A | PC100-322-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 16M x 4 SDRAM |
| HYB 39S256800CT-7.5 | PC133-333-520 | P-TSOP-54-2 (400mil) | 133MHz 4B x 8M x 8 SDRAM |
| HYB 39S256800CT-8 | PC100-222-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 8M x 8 SDRAM |
| HYB 39S256800CT-8A | PC100-322-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 8M x 8 SDRAM |
| HYB 39S256160CT-7.5 | PC133-333-520 | P-TSOP-54-2 (400mil) | 133MHz 4B x 4M x 16 SDRAM |
| HYB 39S256160CT-8 | PC100-222-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 4M x 16 SDRAM |
| HYB 39S256160CT-8A | PC100-322-620 | P-TSOP-54-2 (400mil) | 125MHz 4B x 4M x 16 SDRAM |
| HYB39S256xx0CTL | PC100-xxx-620 | P-TSOP-54-2 (400mil) | Low Power Versions (on request) |

## Pin Description and Pinouts:

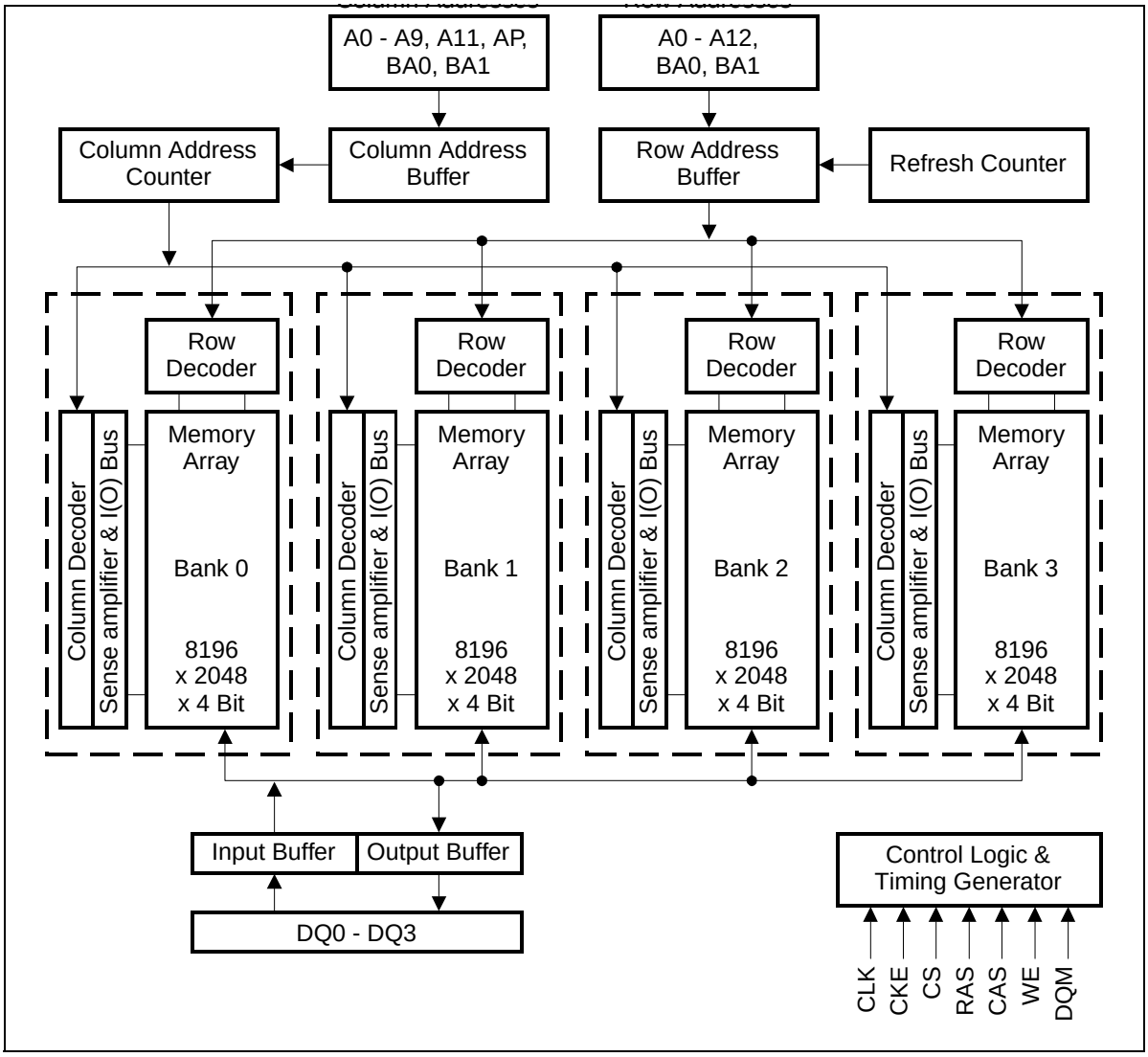
| | | | |
|---|---|---|---|
| **CLK** | Clock Input | **DQ** | Data Input /Output |
| **CKE** | Clock Enable | **DQM, LDQM, UDQM** | Data Mask |
| **$\overline{CS}$** | Chip Select | **Vdd** | Power (+3.3V) |
| **$\overline{RAS}$** | Row Address Strobe | **Vss** | Ground |
| **$\overline{CAS}$** | Column Address Strobe | **Vddq** | Power for DQ's (+ 3.3V) |
| **$\overline{WE}$** | Write Enable | **Vssq** | Ground for DQ's |
| **A0-A12** | Address Inputs | **NC** | not connected |
| **BA0, BA1** | Bank Select | | |


16 M x 16
32 M x 8
64 M x 4
$V_{DD}$ $V_{DD}$ $V_{DD}$ 1 54 $V_{SS}$ $V_{SS}$ $V_{SS}$
DQ0 DQ0 N.C. 2 53 N.C. DQ7 DQ15
$V_{DDQ}$ $V_{DDQ}$ $V_{DDQ}$ 3 52 $V_{SSQ}$ $V_{SSQ}$ $V_{SSQ}$
DQ1 N.C. N.C. 4 51 N.C. N.C. DQ14
DQ2 DQ1 DQ0 5 50 DQ3 DQ6 DQ13
$V_{SSQ}$ $V_{SSQ}$ $V_{SSQ}$ 6 49 $V_{DDQ}$ $V_{DDQ}$ $V_{DDQ}$
DQ3 N.C. N.C. 7 48 N.C. N.C. DQ12
DQ4 DQ2 N.C. 8 47 N.C. DQ5 DQ11
$V_{DDQ}$ $V_{DDQ}$ $V_{DDQ}$ 9 46 $V_{SSQ}$ $V_{SSQ}$ $V_{SSQ}$
DQ5 N.C. N.C. 10 45 N.C. N.C. DQ10
DQ6 DQ3 DQ1 11 44 DQ2 DQ4 DQ9
$V_{SSQ}$ $V_{SSQ}$ $V_{SSQ}$ 12 43 $V_{DDQ}$ $V_{DDQ}$ $V_{DDQ}$
DQ7 N.C. N.C. 13 42 N.C. N.C. DQ8
$V_{DD}$ $V_{DD}$ $V_{DD}$ 14 41 $V_{SS}$ $V_{SS}$ $V_{SS}$
LDQM N.C. N.C. 15 40 N.C. N.C. N.C.
WE WE WE 16 39 DQM DQM UDQM
CAS CAS CAS 17 38 CLK CLK CLK
RAS RAS RAS 18 37 CKE CKE CKE
CS CS CS 19 36 A12 A12 A12
BA0 BA0 BA0 20 35 A11 A11 A11
BA1 BA1 BA1 21 34 A9 A9 A9
A10/AP A10/AP A10/AP 22 33 A8 A8 A8
A0 A0 A0 23 32 A7 A7 A7
A1 A1 A1 24 31 A6 A6 A6
A2 A2 A2 25 30 A5 A5 A5
A3 A3 A3 26 29 A4 A4 A4
$V_{DD}$ $V_{DD}$ $V_{DD}$ 27 28 $V_{SS}$ $V_{SS}$ $V_{SS}$

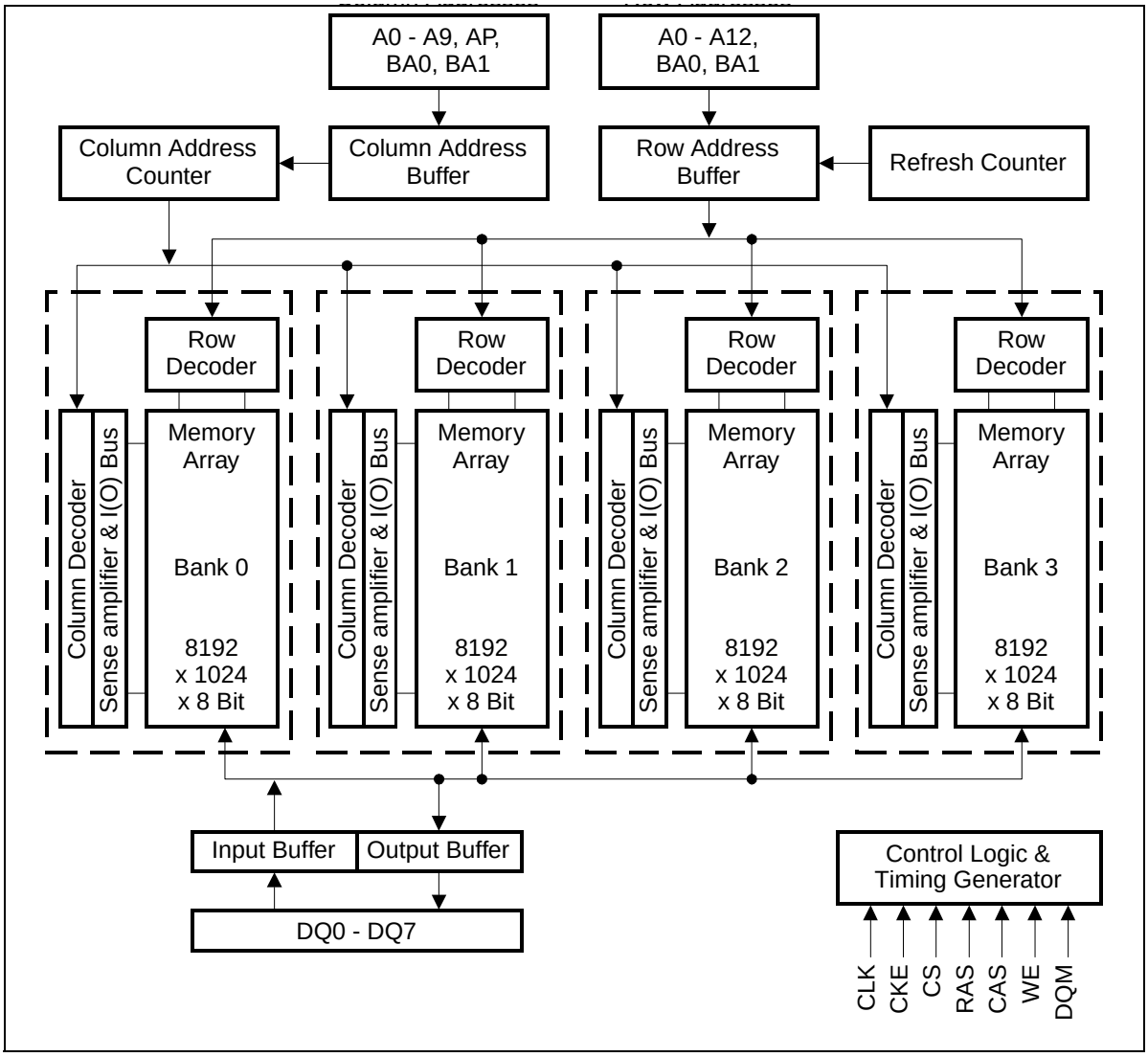
**TSOPII-54 (400 mil x 875 mil, 0.8 mm pitch)**

SPP04126

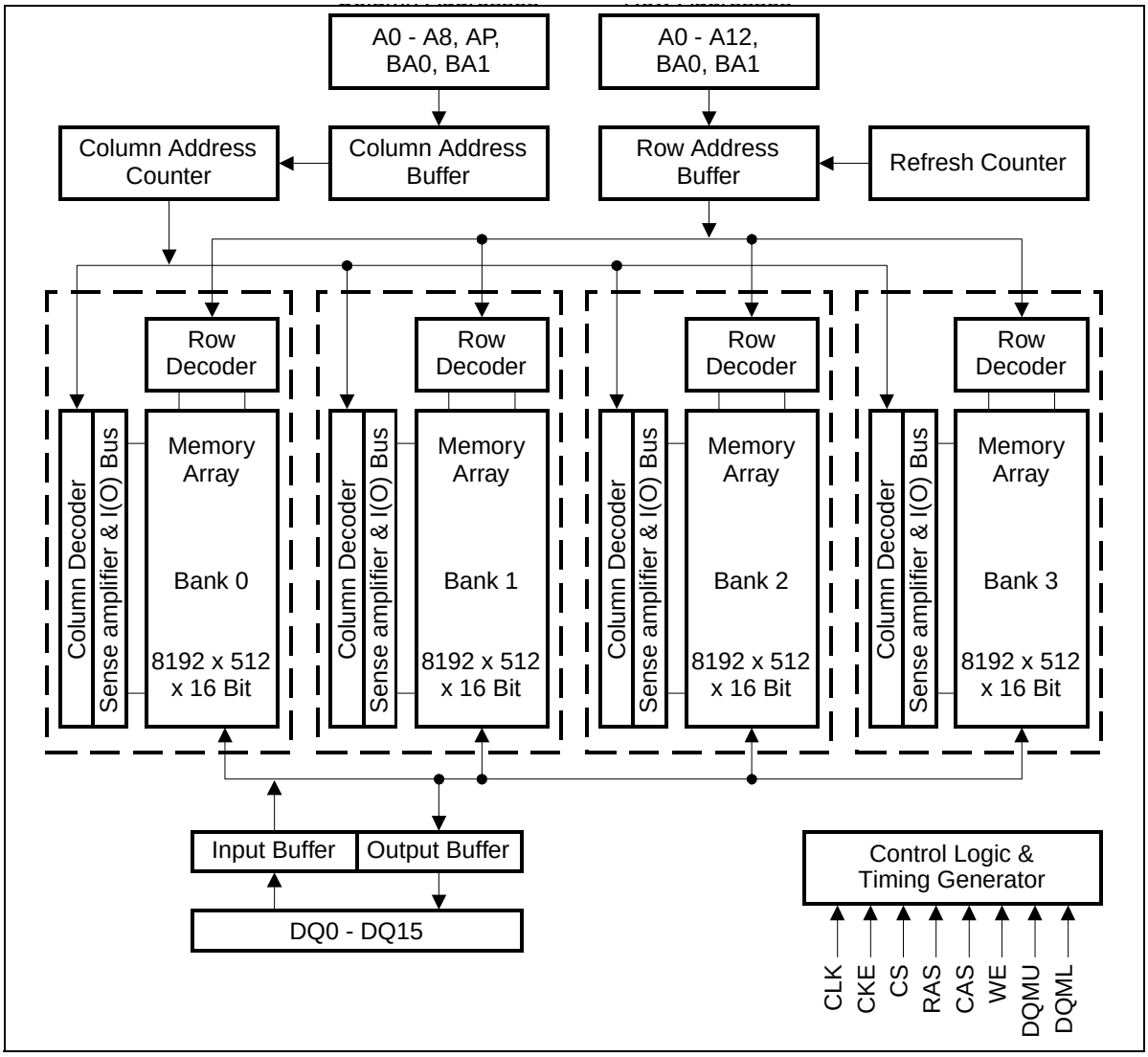
**Pinout for x4, x8 & x16 organised 256M-DRAMs**




**Block Diagram for 64M x 4 SDRAM ( 13 / 11 / 2 addressing)**




**Block Diagram for 32M x 8 SDRAM ( 13 / 10 / 2 addressing)**




**Block Diagram for 16M x16 SDRAM ( 13 / 9 / 2 addressing)**

**Signal Pin Description**

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| CLK | Input | Pulse | Positive Edge | The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock. |
| CKE | Input | Level | Active High | Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode. |
| $\overline{CS}$ | Input | Pulse | Active Low | $\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$<br>$\overline{CAS}$<br>$\overline{WE}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM. |
| A0 - A12 | Input | Level | – | During a Bank Activate command cycle, A0-A12 define the row address (RA0-RA12) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-An define the column address (CA0-CAn) when sampled at the rising clock edge.CAn depends from the SDRAM organization:<br><br>64M x4 SDRAM CAn = CA9, CA11 (Page Length = 2048 bits)<br>32M x8 SDRAM CAn = CA9 (Page Length = 1024 bits)<br>16M x16 SDRAM CAn = CA8 (Page Length = 512 bits)<br><br>In addition to the column address, A10(= AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled.<br>During a Precharge command cycle, A10 (= AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge. |
| BA0, BA1 | Input | Level | – | Bank Select Inputs. Bank address inputs selects which of the four banks a command applies to. |
| DQx | Input Output | Level | – | Data Input/Output pins operate in the same manner as on conventional DRAMs. |

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| DQM<br>LDQM<br>UDQM | Input | Pulse | Active High | The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.<br>One DQM input it present in x4 and x8 SDRAMs, LDQM and UDQM controls the lower and upper bytes in x16 SDRAMs. |
| $V_{DD}$<br>$V_{SS}$ | Supply | – | – | Power and ground for the input buffers and the core logic. |
| $V_{DDQ}$<br>$V_{SSQ}$ | Supply | – | – | Isolated power supply and ground for the output buffers to provide improved noise immunity. |

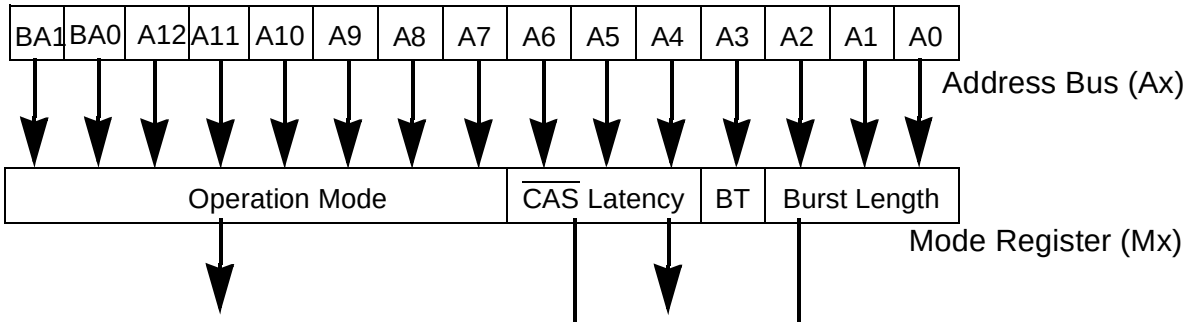
## Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

| Operation | Device State | CKE n-1 | CKE n | DQM | BA0 BA1 | AP= A10 | Addr. | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Bank Active | Idle[3] | H | X | X | V | V | V | L | L | H | H |
| Bank Precharge | Any | H | X | X | V | L | X | L | L | H | L |
| Precharge All | Any | H | X | X | X | H | X | L | L | H | L |
| Write | Active[3] | H | X | X | V | L | V | L | H | L | L |
| Write with Autoprecharge | Active[3] | H | X | X | V | H | V | L | H | L | L |
| Read | Active[3] | H | X | X | V | L | V | L | H | L | H |
| Read with Autoprecharge | Active[3] | H | X | X | V | H | V | L | H | L | H |
| Mode Register Set | Idle | H | X | X | V | V | V | L | L | L | L |
| No Operation | Any | H | X | X | X | X | X | L | H | H | H |
| Burst Stop | Active | H | X | X | X | X | X | L | H | H | L |
| Device Deselect | Any | H | X | X | X | X | X | H | X | X | X |
| Auto Refresh | Idle | H | H | X | X | X | X | L | L | L | H |
| Self Refresh Entry | Idle | H | L | X | X | X | X | L | L | L | H |
| Self Refresh Exit | Idle (Self Refr.) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | X |
| Clock Suspend Entry | Active | H | L | X | X | X | X | X | X | X | X |
| Power Down Entry (Precharge or active standby) | Idle Active[4] | H | L | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | X |
| Clock Suspend Exit | Active | L | H | X | X | X | X | X | X | X | X |
| Power Down Exit | Any (Power Down) | L | H | X | X | X | X | H | X | X | X |
| | | | | | | | | L | H | H | L |
| Data Write/Output Enable | Active | H | X | L | X | X | X | X | X | X | X |
| Data Write/Output Disable | Active | H | X | H | X | X | X | X | X | X | X |

## Notes

1. V = Valid, x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. This is the state of the banks designated by BA0, BA1 signals.
4. Power Down Mode can't be entered in a burst cycle. When this command assert in the burst mode cycle device is clock suspend mode.




**Operation Mode**

| M9 | Mode |
|---|---|
| 0 | burst read / burst write |
| 1 | burst read / single write |

**Burst Type**

| M3 | Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

**$\overline{\text{CAS}}$ Latency**

| M6 | M5 | M4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

**Burst Length**

| M2 | M1 | M0 | Length | |
|---|---|---|---|---|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | Full page *) | |

*) optional feature on this device

**Power On and Initialization**

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner.During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

**Programming the Mode Register**

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a $\overline{\text{CAS}}$ **Latency** Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

**Read and Write Operation**

When $\overline{\text{RAS}}$ is low and both $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high at the positive edge of the clock, a $\overline{\text{RAS}}$ cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A $\overline{\text{CAS}}$ cycle is triggered by setting $\overline{\text{RAS}}$ high and $\overline{\text{CAS}}$ low at a clock timing after a necessary delay, $t_{RCD}$, from the $\overline{\text{RAS}}$ timing. $\overline{\text{WE}}$ is used to define either a read ($\overline{\text{WE}}$ = H) or a write ($\overline{\text{WE}}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single $\overline{\text{CAS}}$ cycle, serial data read or write operations are allowed at up to a 133 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page, where full page is an optional feature on this device. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the $\overline{\text{CAS}}$ timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do nor self terminate once the burst length has been reached. In other words, unlike burst length of 2, 4 or 8, full page burst

continues until it is terminated using other commands. Full page operation is an optional feature on this device, which is built in by design, but not tested on every component.

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the $\overline{RAS}$ cycle latches the sense amplifiers. The maximum $t_{RAS}$ or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be performed between different pages.

**Burst Length and Sequence:**

| Burst Length | Starting Address (A2 A1 A0) | Sequential Burst Addressing (decimal) | Interleave Burst Addressing (decimal) |
|---|---|---|---|
| 2 | xx0<br>xx1 | 0, 1<br>1, 0 | 0, 1<br>1, 0 |
| 4 | x00<br>x01<br>x10<br>x11 | 0, 1, 2, 3<br>1, 2, 3, 0<br>2, 3, 0, 1<br>3, 0, 1, 2 | 0, 1, 2, 3<br>1, 0, 3, 2<br>2, 3, 0, 1<br>3, 2, 1, 0 |
| 8 | 000<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | 0 1 2 3 4 5 6 7<br>1 2 3 4 5 6 7 0<br>2 3 4 5 6 7 0 1<br>3 4 5 6 7 0 1 2<br>4 5 6 7 0 1 2 3<br>5 6 7 0 1 2 3 4<br>6 7 0 1 2 3 4 5<br>7 0 1 2 3 4 5 6 | 0 1 2 3 4 5 6 7<br>1 0 3 2 5 4 7 6<br>2 3 0 1 6 7 4 5<br>3 2 1 0 7 6 5 4<br>4 5 6 7 0 1 2 3<br>5 4 7 6 1 0 3 2<br>6 7 4 5 2 3 0 1<br>7 6 5 4 3 2 1 0 |
| Full Page (optional) | nnn | Cn, Cn+1, Cn+2 | not supported |

**Refresh Mode**

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic

refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. The mode restores the word lines after $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

**DQM Function**

DQM has two functions for data I/O read and write operations. During reads, when it turns to „high“ at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency $t_{DQZ}$). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency $t_{DQW}$ = zero clocks).

**Suspend Mode**

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency $t_{CSL}$).

**Power Down**

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE „high“. One clock delay is required for power down mode entry and and exit.

**Auto Precharge**

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the $\overline{CAS}$ timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. If CA10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to $t_{WR}$ (“write recovery time”) after the last data in.

**Precharge Command**

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for $\overline{CAS}$ latency = 2 and two clocks before the last data out for $\overline{CAS}$ latency = 3. Writes require a time delay twr (“write recovery time”) of 2 clocks minimum from the last data out to apply the precharge command.

Bank Selection by Address Bits

| A10 | BA0 | BA1 | |
|---|---|---|---|
| 0 | 0 | 0 | Bank 0 |
| 0 | 0 | 1 | Bank 1 |
| 0 | 1 | 0 | Bank 2 |
| 0 | 1 | 1 | Bank 3 |
| 1 | x | x | all Banks |

**Burst Termination**

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

### Absolute Maximum Ratings

Operating temperature range .....0 to + 70 °C
Storage temperature range.....– 55 to + 150 °C
Input/output voltage .....– 0.3 to Vdd+0.3 V
Power supply voltage $V_{DD}$ / $V_{DDQ}$ ..... – 0.3 to + 4.6 V
Power Dissipation..... .....1 W
Data out current (short circuit) ..... 50 mA

**Note:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### Recommended Operation and Characteristics:

$T_A$ = 0 to 70 °C; $V_{SS}$ = 0 V; $V_{DD,}V_{DDQ}$ = 3.3 V ± 0.3 V

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Input high voltage | $V_{IH}$ | 2.0 | Vdd+0.3 | V | 1, 2 |
| Input low voltage | $V_{IL}$ | – 0.3 | 0.8 | V | 1, 2 |
| Output high voltage ($I_{OUT}$ = – 4.0 mA) | $V_{OH}$ | 2.4 | – | V | 3 |
| Output low voltage ($I_{OUT}$ = 4.0 mA) | $V_{OL}$ | – | 0.4 | V | 3 |
| Input leakage current, any input (0 V < $V_{IN}$ < Vddq, all other inputs = 0 V) | $I_{I(L)}$ | – 5 | 5 | µA | |
| Output leakage current (DQ is disabled, 0 V < $V_{OUT}$ < $V_{dd}$) | $I_{O(L)}$ | – 5 | 5 | µA | |

**Notes:**

1. All voltages are referenced to VSS.
2. Vih may overshoot to Vdd + 2.0 V for pulse width of < 4ns with 3.3V. Vil may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

### Capacitance

$T_A$ = 0 to 70 °C; $V_{DD}$ = 3.3 V ± 0.3 V, $f$ = 1 MHz

| Parameter | Symbol | Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Input capacitance (CLK) | $C_{I1}$ | 2.5 | 3.5 | pF |
| Input capacitance (A0-A12, BA0,BA1,$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM) | $C_{I2}$ | 2.5 | 3.8 | pF |
| Input / Output capacitance (DQ) | $C_{IO}$ | 4.0 | 6.0 | pF |

**Operating Currents** ($T_A$ = 0 to 70°C, Vdd = 3.3V ± 0.3V

(Recommended Operating Conditions unless otherwise noted)

| Parameter & Test Condition | | Symb. | -7.5 | -8/-8A | | Note |
|---|---|---|---|---|---|---|
| | | | max. | max. | | |
| **OPERATING CURRENT**<br>tck=tckmin,<br>All banks operated in random access,<br>all banks operated in ping-pong manner. | | ICC1 | 230 | 170 | mA | 3, 4 |
| **PRECHARGE STANDBY CURRENT in Power Down Mode**<br>$\overline{CS}$ =VIH (min.), CKE<=Vil(max) | tck = min. | ICC2P | 2 | 2 | mA | 3 |
| **PRECHARGE STANDBY CURRENT in Non-Power Down Mode**<br>$\overline{CS}$ = VIH (min.), CKE>=Vih(min) | tck = min. | ICC2N | 40 | 30 | mA | 3 |
| **NO OPERATING CURRENT**<br>tck = min., $\overline{CS}$ = VIH(min),<br>active state ( max. 4 banks) | CKE>=VIH(min.) | ICC3N | 50 | 45 | mA | 3 |
| | CKE<=VIL(max.) | ICC3P | 10 | 10 | mA | 3 |
| **BURST OPERATING CURRENT**<br>tck = min.,<br>Read command cycling | | ICC4 | 150 | 100 | mA | 3,4 |
| **AUTO REFRESH CURRENT**<br>tck = min., trc=trcmin.,<br>Auto Refresh command cycling | | ICC5 | 240 | 220 | mA | 3 |
| **SELF REFRESH CURRENT**<br>Self Refresh Mode, CKE=0.2V<br>tck=infinity | standard version | ICC6 | 3 | 3 | mA | |
| | L-version | | 1.7 | 1.7 | mA | |

**Notes:**

3. These parameters depend on the cycle rate. All values are measured at 133 MHz operation frequency for -7.5 devices and at 100 MHz for -8/-8A devices.
   Input signals are changed once during tck.
4. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the VDDQ current is excluded.

**AC Characteristics** 1)2)
$T_A$ = 0 to 70 °C; $V_{SS}$ = 0 V; $Vdd$ = 3.3 V ± 0.3 V, $t_T$ = 1 ns

| Parameter | Symbol | Limit Values | | | | | | Unit | |
|---|---|---|---|---|---|---|---|---|---|
| | | -7.5 PC133-333 | | -8 PC100-222 | | -8A PC100-322 | | | |
| | | min. | max. | min. | max. | min. | max. | | |
| ***Clock and Clock Enable*** | | | | | | | | | |
| Clock Cycle Time | | | | | | | | | |
| $\overline{\text{CAS}}$ Latency = 3 | $t_{CK}$ | 7.5 | | 8 | – | 8 | – | ns | |
| $\overline{\text{CAS}}$ Latency = 2 | | 10 | | 10 | – | 12 | – | ns | |
| Clock Frequency | | | | | | | | | |
| $\overline{\text{CAS}}$ Latency = 3 | $t_{CK}$ | – | 133 | – | 125 | – | 125 | MHz | |
| $\overline{\text{CAS}}$ Latency = 2 | | – | 100 | – | 100 | – | 83 | MHz | |
| Access Time from Clock | | | | | | | | | |
| $\overline{\text{CAS}}$ Latency = 3 | $t_{AC}$ | – | 5.4 | – | 6 | – | 6 | ns | 2, 3, 7 |
| $\overline{\text{CAS}}$ Latency = 2 | | – | 6 | – | 6 | – | 6 | ns | |
| Clock High Pulse Width | $t_{CH}$ | 2.5 | – | 3 | – | 3 | – | ns | |
| Clock Low Pulse Width | $t_{CL}$ | 2.5 | – | 3 | – | 3 | – | ns | |
| Transition time | $t_T$ | 0.3 | 1.2 | 0.5 | 10 | 0.5 | 10 | ns | |
| ***Setup and Hold Times*** | | | | | | | | | |
| Input Setup Time | $t_{IS}$ | 1.5 | – | 2 | – | 2 | – | ns | 4 |
| Input Hold Time | $t_{IH}$ | 0.8 | – | 1 | – | 1 | – | ns | 4 |
| CKE Setup Time | $t_{CKS}$ | 1.5 | – | 2 | – | 2 | – | ns | 4 |
| CKE Hold Time | $t_{CKH}$ | 0.8 | – | 1 | – | 1 | – | ns | 4 |
| Mode Register set to Active delay | $t_{RSC}$ | 2 | – | 2 | – | 2 | – | CLK | |
| Power Down Mode Entry Time | $t_{SB}$ | 0 | 7.5 | 0 | 8 | 0 | 8 | ns | |
| ***Common Parameters*** | | | | | | | | | |
| Row to Column Delay Time | $t_{RCD}$ | 20 | – | 20 | – | 20 | | ns | 5 |
| Row Precharge Time | $t_{RP}$ | 20 | – | 20 | – | 20 | | ns | 5 |
| Row Active Time | $t_{RAS}$ | 45 | 100k | 48 | 100k | 48 | 100k | ns | 5 |
| Row Cycle Time | $t_{RC}$ | 67 | – | 70 | – | 70 | – | ns | 5 |

| Parameter | Symbol | Limit Values | | | | | | Unit | |
|---|---|---|---|---|---|---|---|---|---|
| | | -7.5 PC133-333 | | -8 PC100-222 | | -8A PC100-322 | | | |
| | | min. | max. | min. | max. | min. | max. | | |
| Activate(a) to Activate(b) Command period | $t_{RRD}$ | 15 | – | 16 | – | 16 | | ns | 5 |
| $\overline{CAS}$(a) to $\overline{CAS}$(b) Command period | $t_{CCD}$ | 1 | – | 1 | – | 1 | – | CLK | |
| ***Refresh Cycle*** | | | | | | | | | |
| Refresh Period (8192 cycles) | $t_{REF}$ | – | 64 | – | 64 | – | 64 | ms | |
| Self Refresh Exit Time | $t_{SREX}$ | 1 | – | 1 | | 1 | | CLK | 6 |
| ***Read Cycle*** | | | | | | | | | |
| Data Out Hold Time | $t_{OH}$ | 3 | – | 3 | – | 3 | – | ns | 2, 7 |
| Data Out to Low Impedance Time | $t_{LZ}$ | 0 | – | 0 | – | 0 | – | ns | |
| Data Out to High Impedance Time | $t_{HZ}$ | 3 | 7 | 3 | 8 | 3 | 8 | ns | |
| DQM Data Out Disable Latency | $t_{DQZ}$ | – | 2 | – | 2 | – | 2 | CLK | |
| ***Write Cycle*** | | | | | | | | | |
| Data Input to Precharge (write recovery) | $t_{WR}$ | 2 | – | 2 | – | 2 | – | CLK | 8 |
| DQM Write Mask Latency | $t_{DQW}$ | 0 | – | 0 | – | 0 | – | CLK | |

## Notes for AC Parameters:

1. For proper power-up see the operation section of this data sheet.
2. AC timing tests have $V_{il}$ = 0.4 V and $V_{ih}$ = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is meas ured between $V_{ih}$ and $V_{il}$. All AC measurements assume $t_T$=1ns with the AC output load circuit shown in fig.1.Specified tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.

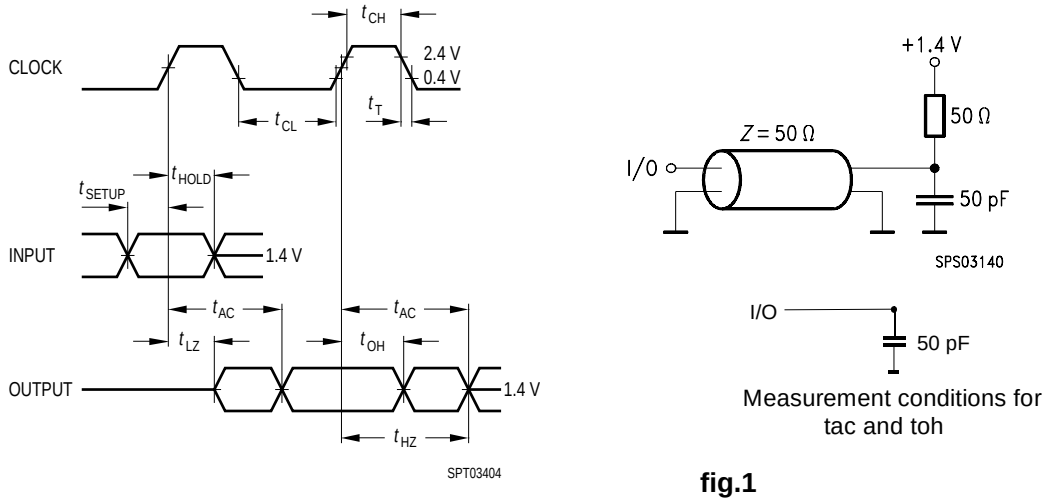
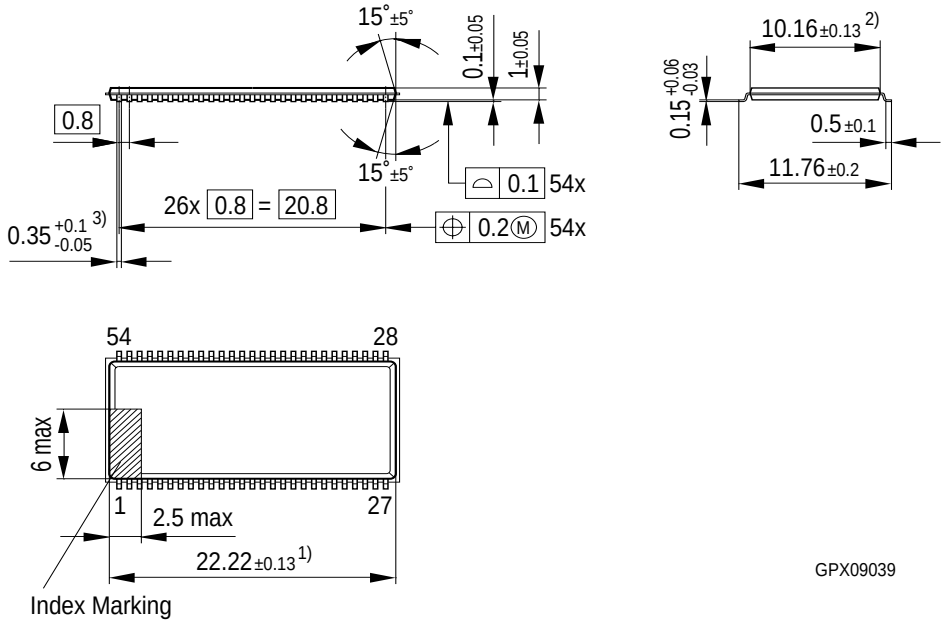



**fig.1**

3. If clock rising time is longer than 1 ns, a time ($t_T$/2 - 0.5) ns has to be added to this parameter.
4. If tT is longer than 1 ns, a time ($t_T$ -1) ns has to be added to this parameter.
5. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
   *the number of clock cycle = specified value of timing period (counted in fractions as a whole number)*
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.
7. Access time from clock tac is 4.6 ns for PC133 components with no termination and 0 pF load,
   Data out hold time toh is 1.8 ns for PC133 components with no termination and 0 pF load.
8. The write recovery time twr = 2 CLK cycles is a digital interlock on this device. Special devices with twr = 1 CLK for operations at less or equal 83 MHz will be available.

## Package Outlines

**Plastic Package P-TSOPII-54**
(400 mil, 0.8 mm lead pitch)
Thin Small Outline Package, SMD

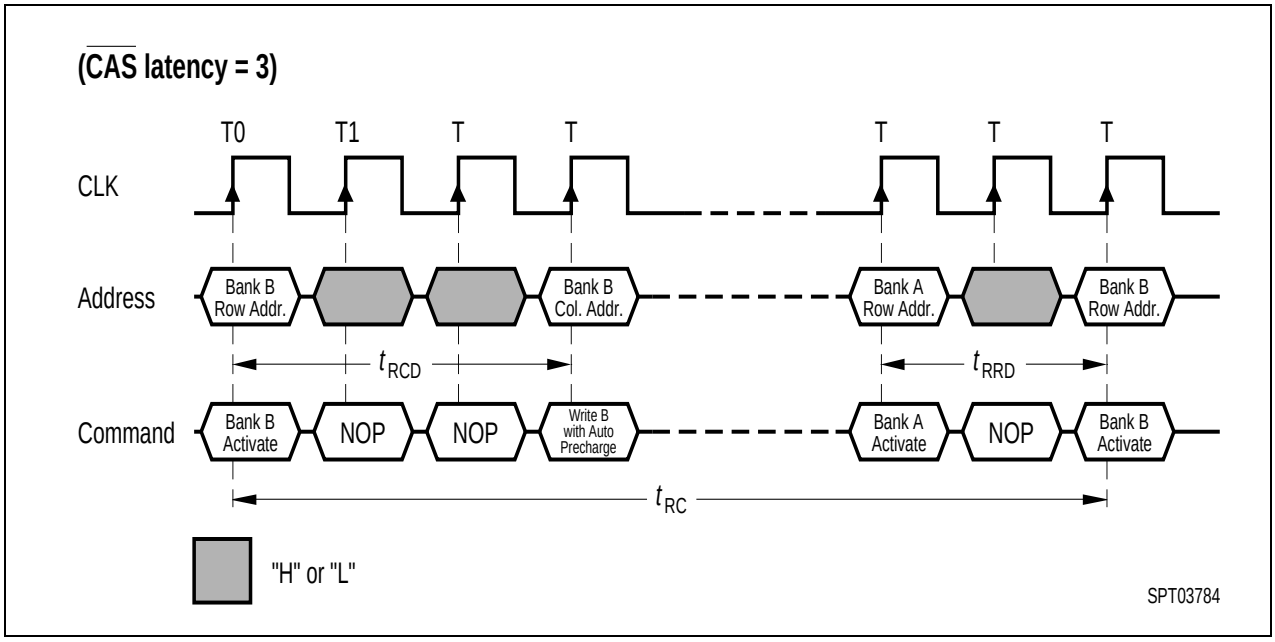



1) Does not include plastic or metal protrusion of 0.15 max per side
2) Does not include plastic protrusion of 0.25 max per side
3) Does not include dambar protrusion of 0.13 max per side

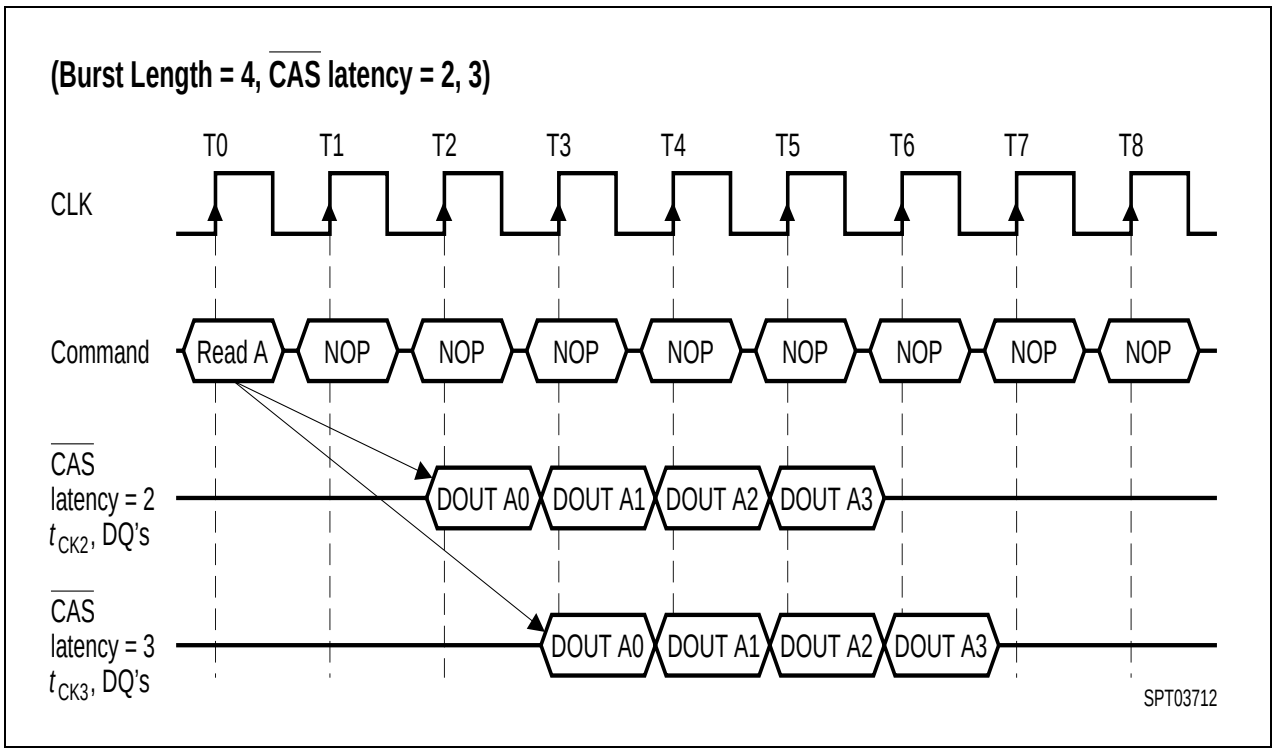
## Timing Diagrams

1. Bank Activate Command Cycle
2. Burst Read Operation
3. Read Interrupted by a Read
4. Read to Write Interval
    4.1 Read to Write Interval
    4.2 Minimum Read to Write Interval
    4.3 Non-Minimum Read to Write Interval
5. Burst Write Operation
6. Write and Read Interrupt
    6.1 Write Interrupted by a Write
    6.2 Write Interrupted by Read
7. Burst Write & Read with Auto-Precharge
    7.1 Burst Write with Auto-Precharge
    7.2 Burst Read with Auto-Precharge
8. AC- Parameters
    8.1 AC Parameters for a Write Timing
    8.2 AC Parameters for a Read Timing
9. Mode Register Set
10. Power on Sequence and Auto Refresh (CBR)
11. Clock Suspension (using CKE)
    11. 1 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 2
    11. 2 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 3
    11. 3 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 2
    11. 4 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 3
12. Power Down Mode and Clock Suspend
13. Self Refresh ( Entry and Exit )
14. Auto Refresh ( CBR )
15. Random Column Read ( Page within same Bank)
    15.1 $\overline{\text{CAS}}$ Latency = 2
    15.2 $\overline{\text{CAS}}$ Latency = 3
16. Random Column Write ( Page within same Bank)
    16.1 $\overline{\text{CAS}}$ Latency = 2
    16.2 $\overline{\text{CAS}}$ Latency = 3
17. Random Row Read ( Interleaving Banks) with Precharge
    17.1 $\overline{\text{CAS}}$ Latency = 2
    17.2 $\overline{\text{CAS}}$ Latency = 3
18. Random Row Write ( Interleaving Banks) with Precharge
    18.1 $\overline{\text{CAS}}$ Latency = 2
    18.2 $\overline{\text{CAS}}$ Latency = 3
19. Precharge Termination of a Burst

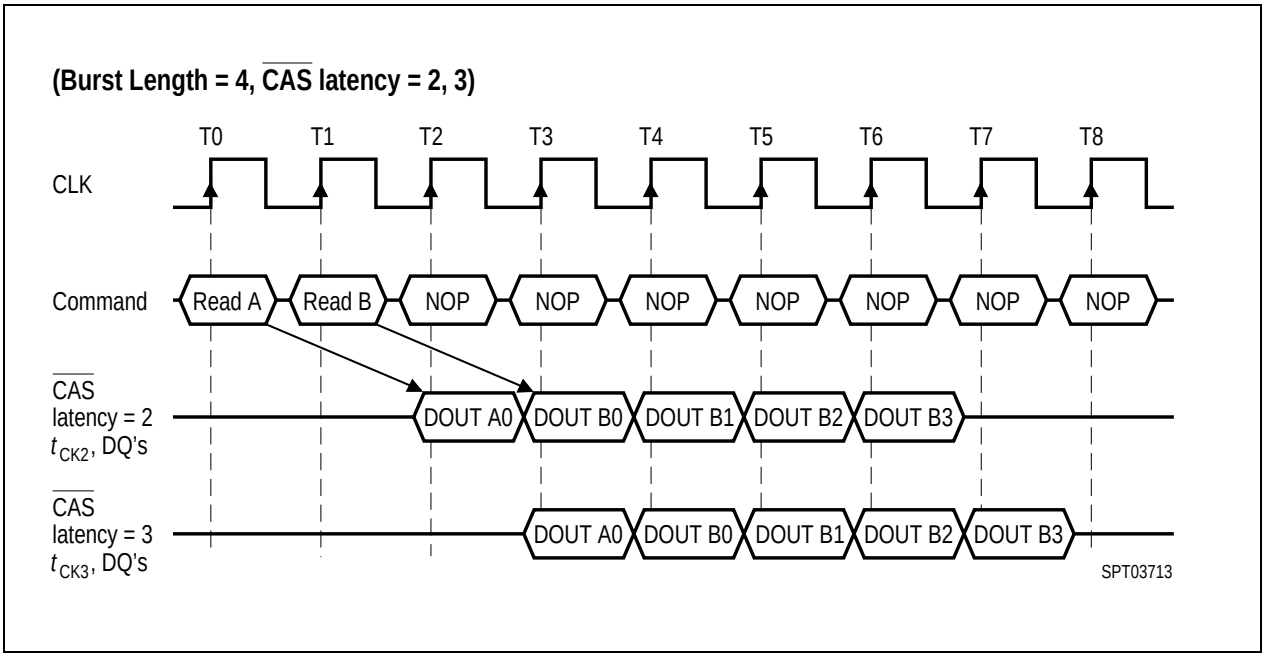
## 1. Bank Activate Command Cycle




## 2. Burst Read Operation

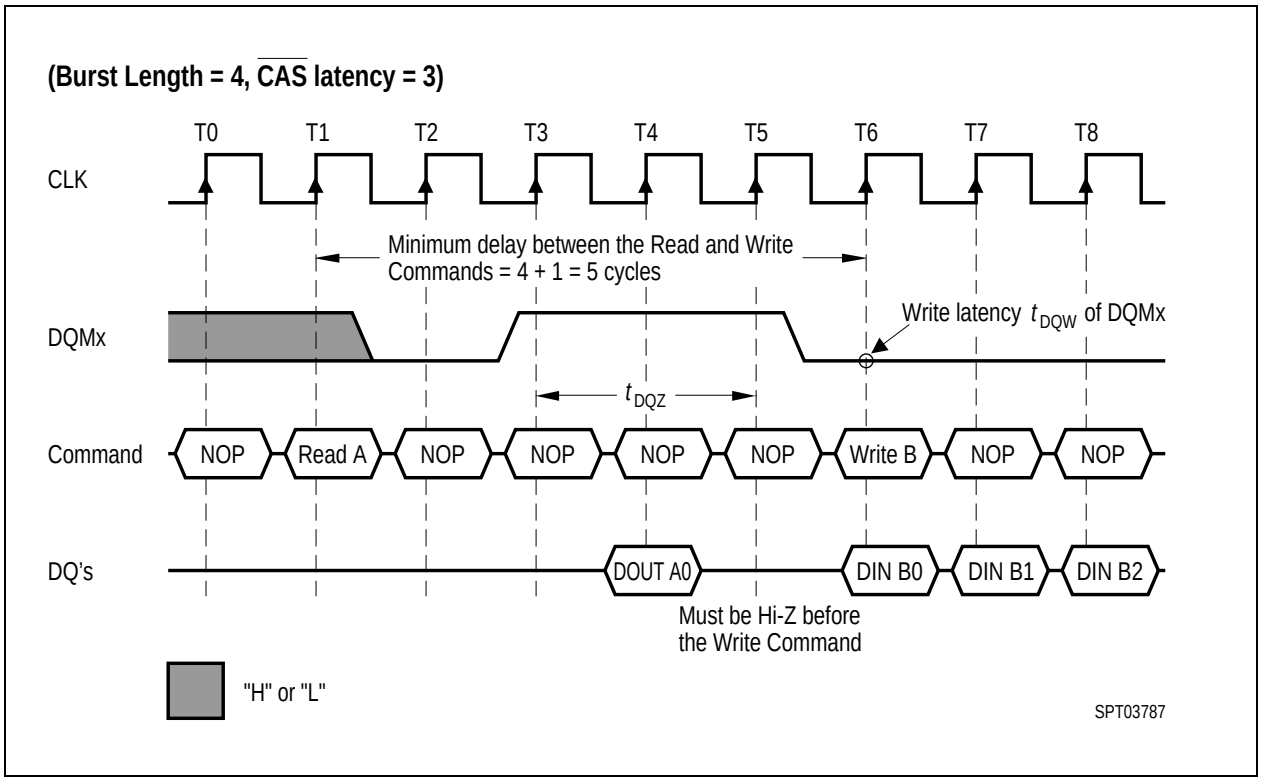


## 3. Read Interrupted by a Read

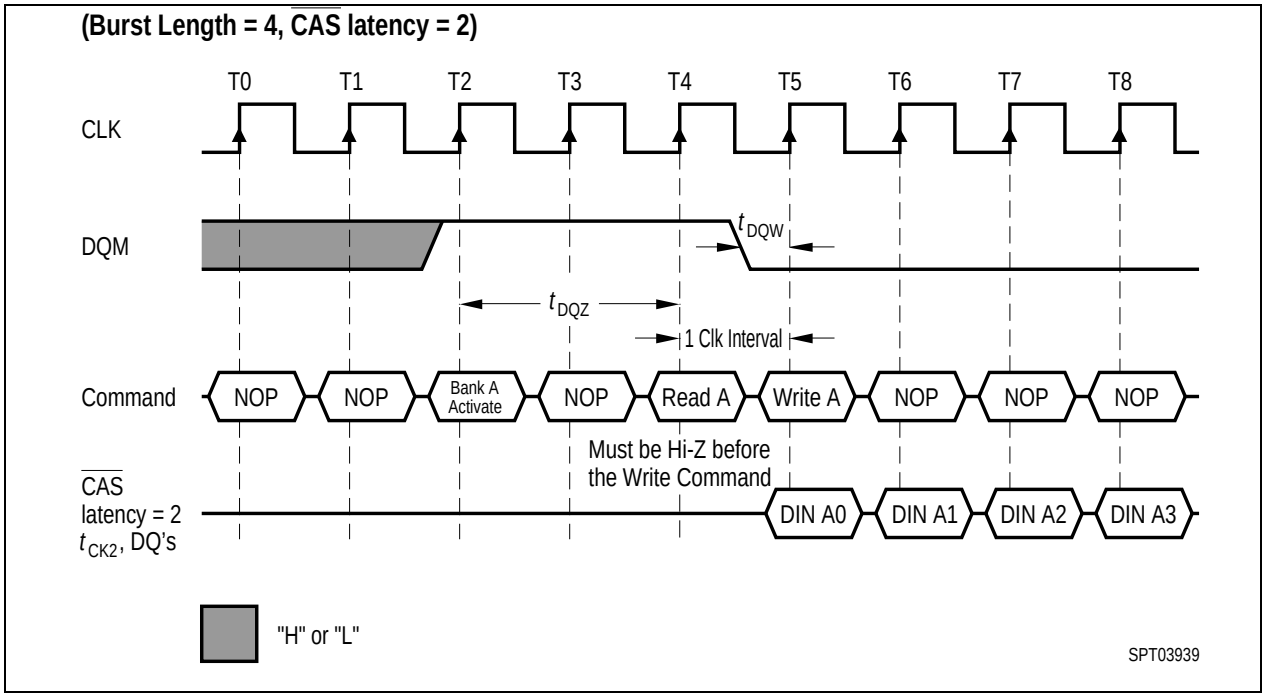



## 4. Read to Write Interval

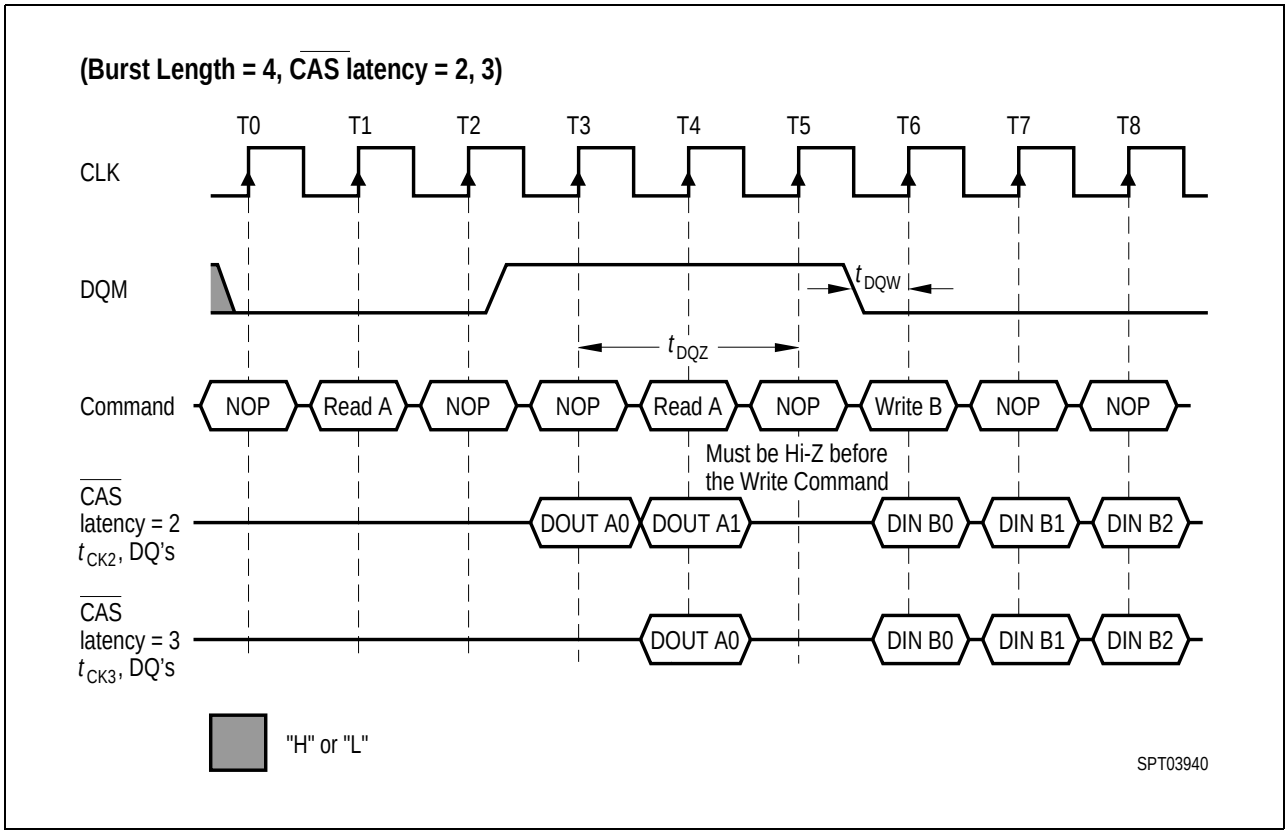
### 4.1 Read to Write Interval



## 4 2. Minimum Read to Write Interval

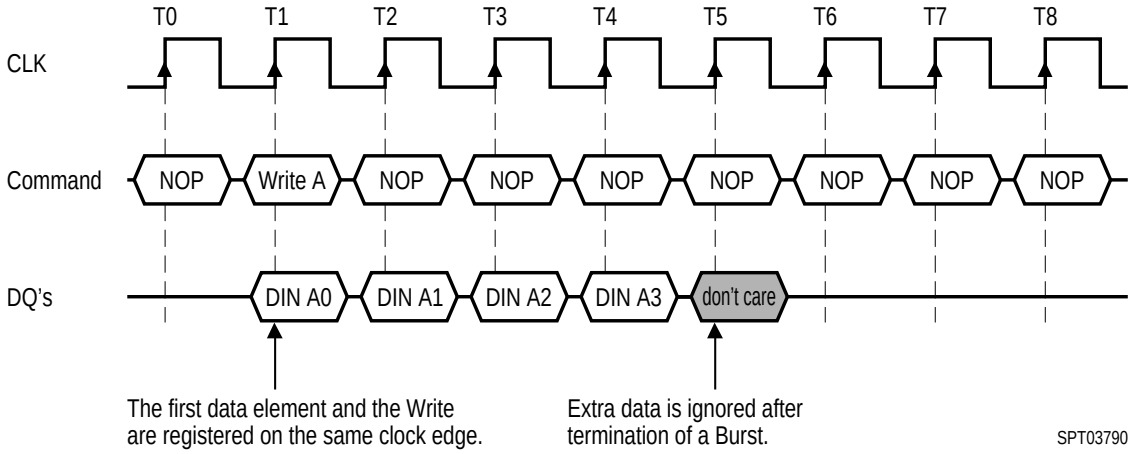



## 4. 3. Non-Minimum Read to Write Interval



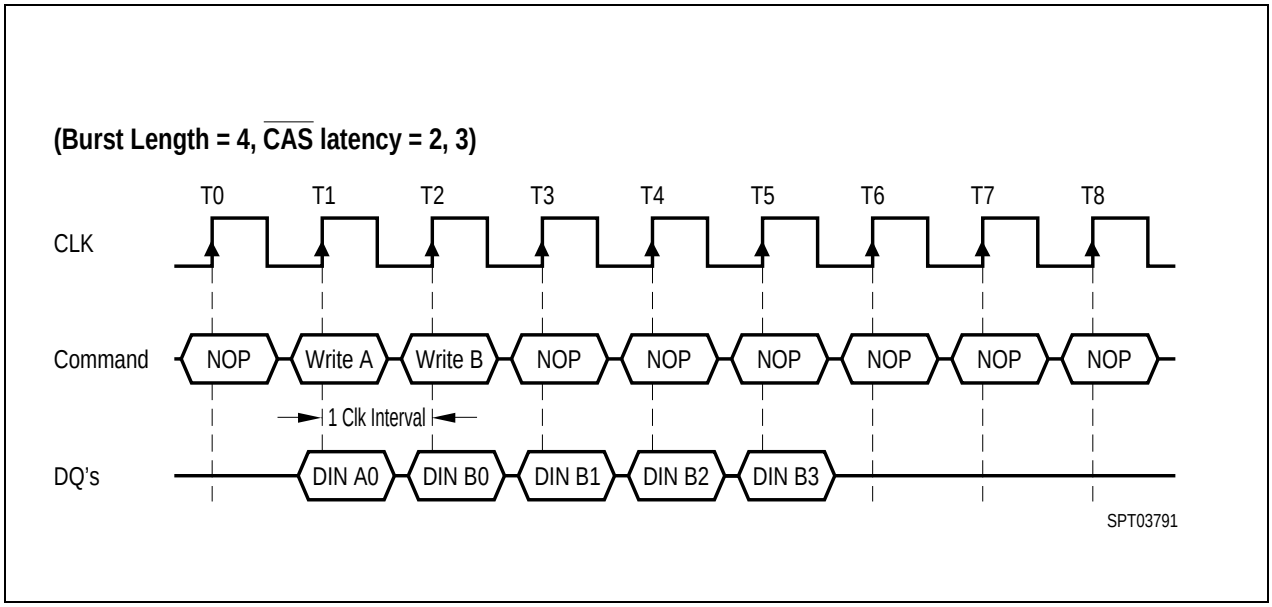
## 5. Burst Write Operation

(

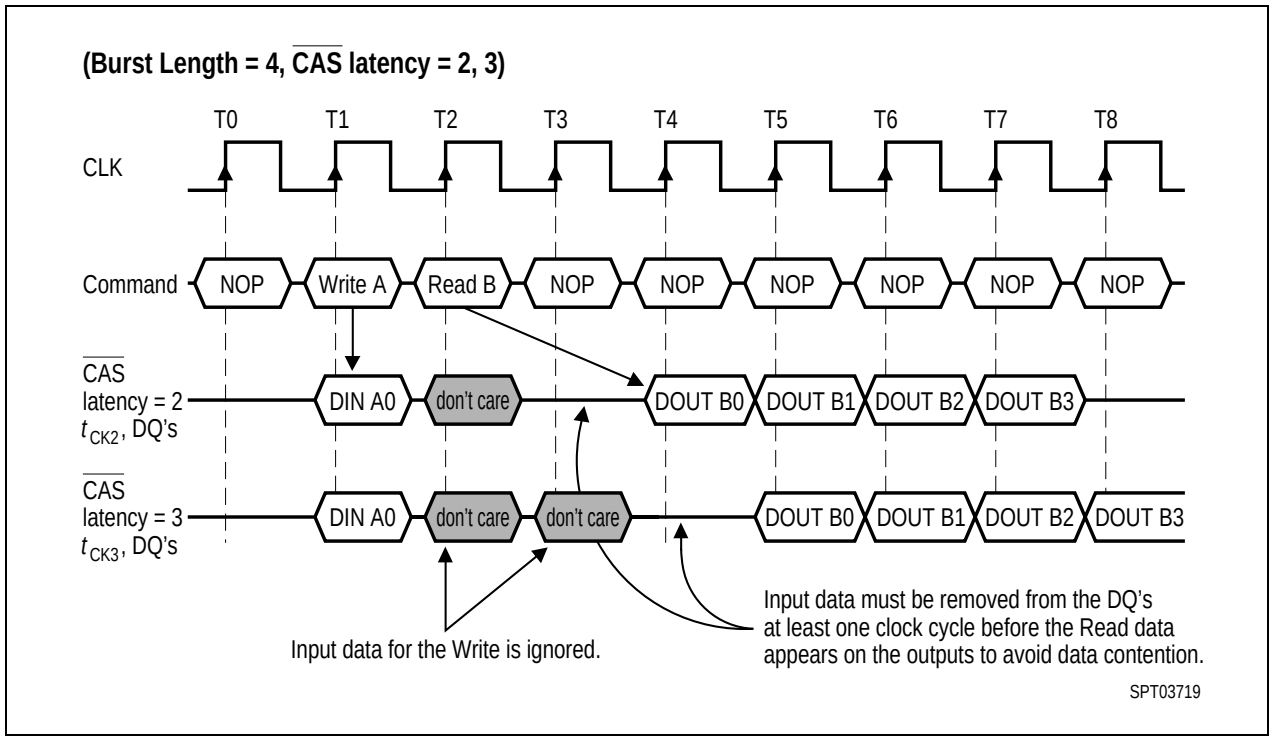


# 6. Write and Read Interrupt

## 6.1 Write Interrupted by a Write

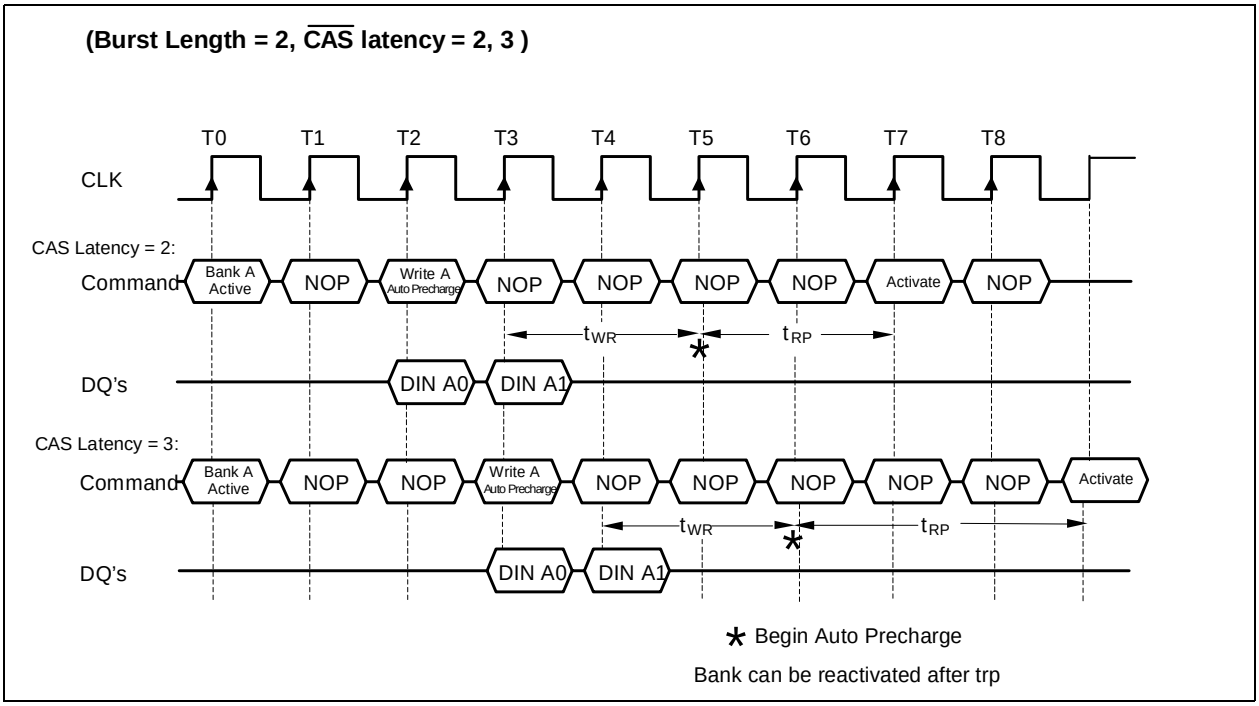



## 6.2 Write Interrupted by a Read

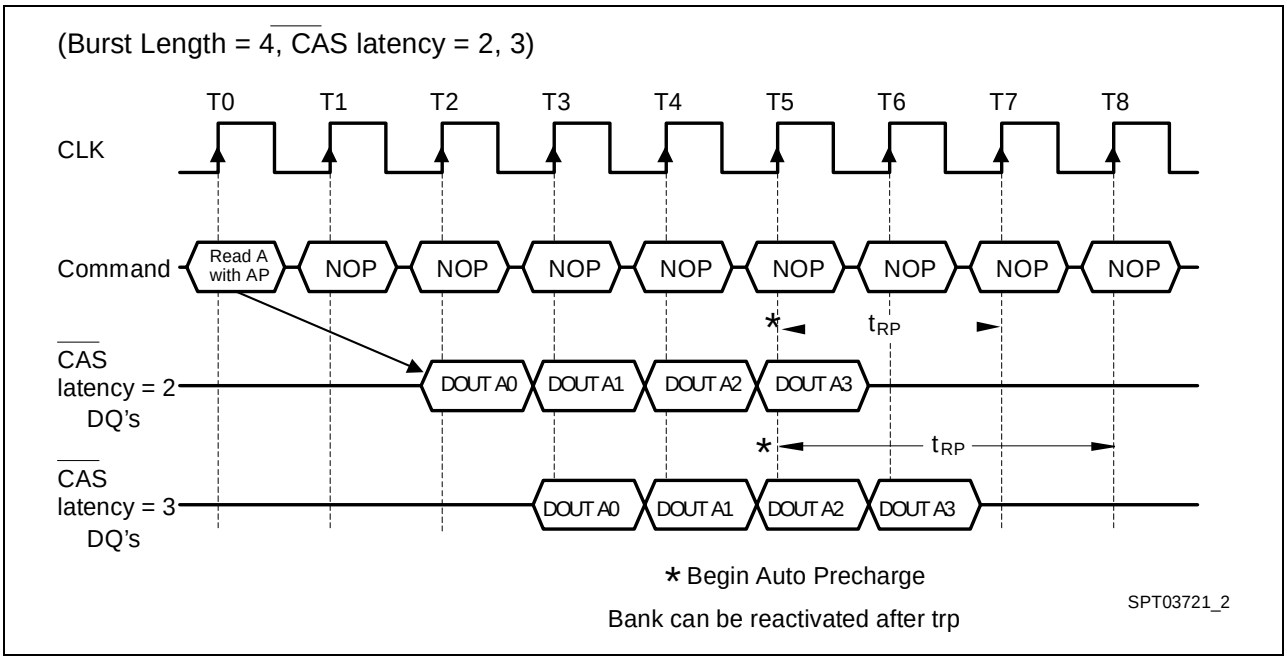


# 7. Burst Write and Read with Auto Precharge

## 7.1 Burst Write with Auto-Precharge

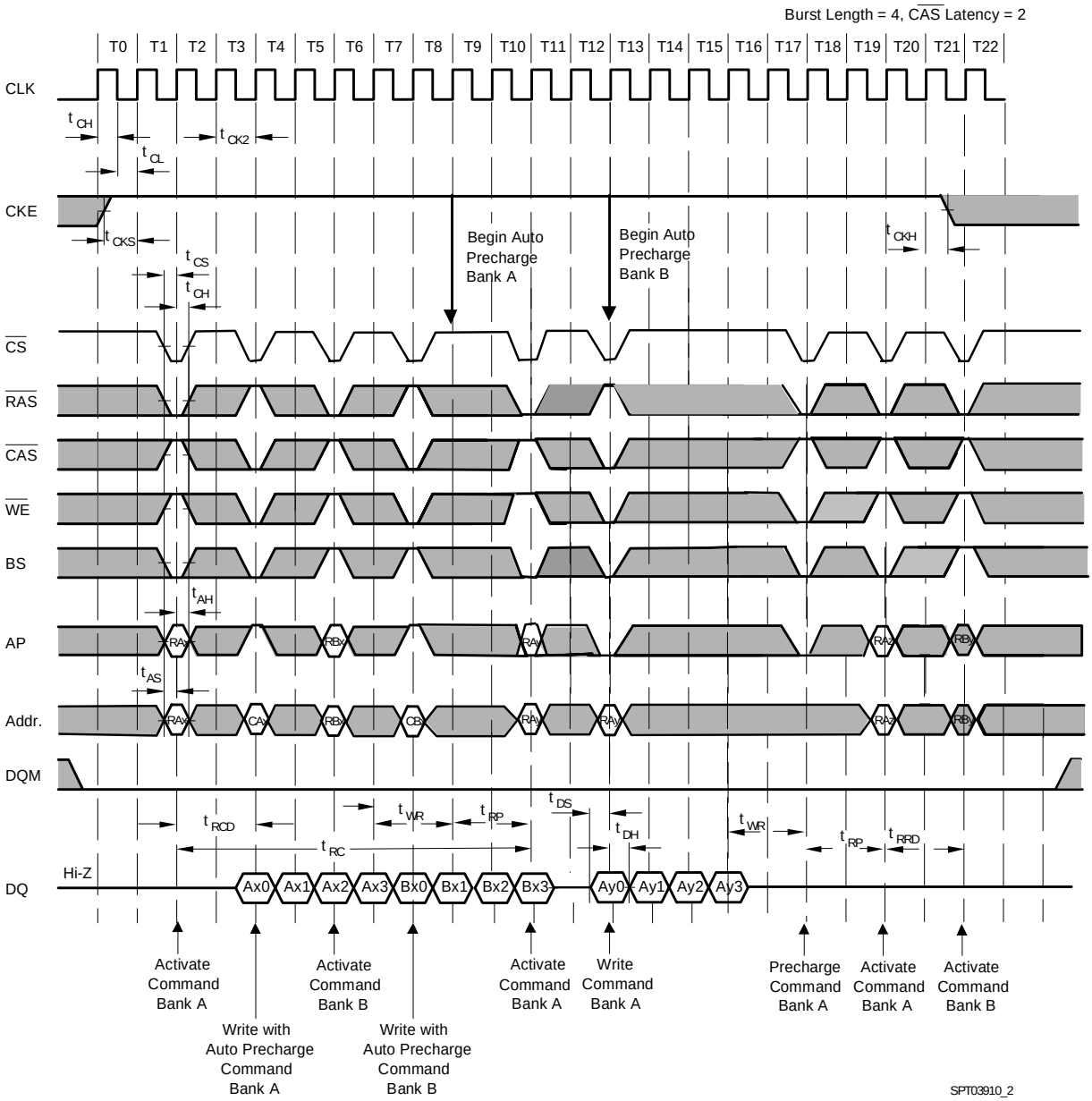



## 7.2 Burst Read with Auto-Precharge

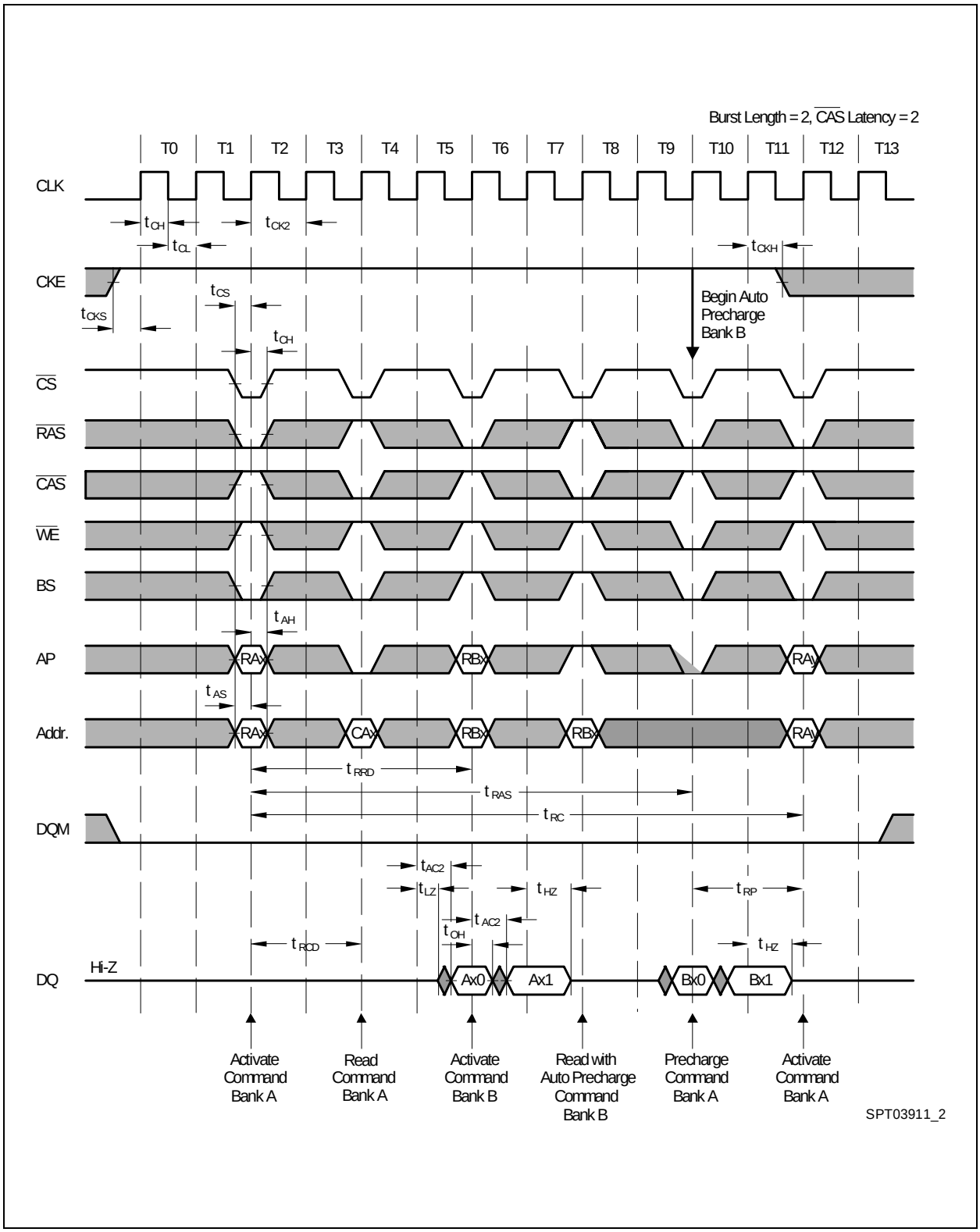


# 8. AC Parameters

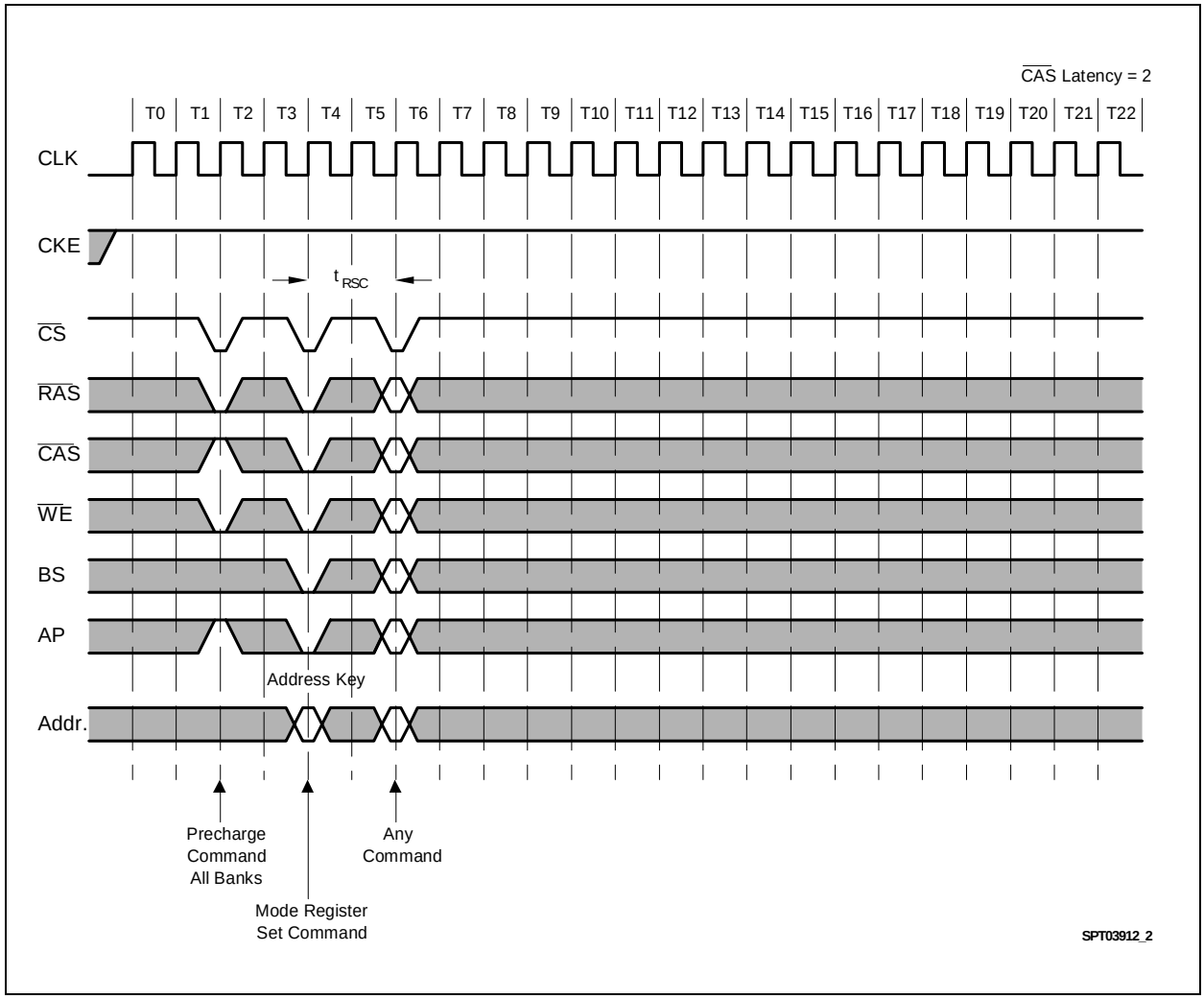
## 8.1 AC Parameters for a Write Timing


Burst Length = 4, CAS Latency = 2
T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22
CLK
CKE
CS
RAS
CAS
WE
BS
AP
Addr.
DQM
DQ
Hi-Z
Begin Auto Precharge Bank A
Begin Auto Precharge Bank B
Ax0 Ax1 Ax2 Ax3 Bx0 Bx1 Bx2 Bx3 Ay0 Ay1 Ay2 Ay3
Activate Command Bank A
Write with Auto Precharge Command Bank A
Activate Command Bank B
Write with Auto Precharge Command Bank B
Activate Command Bank A
Write Command Bank A
Precharge Command Bank A
Activate Command Bank A
Activate Command Bank B
SPT03910_2

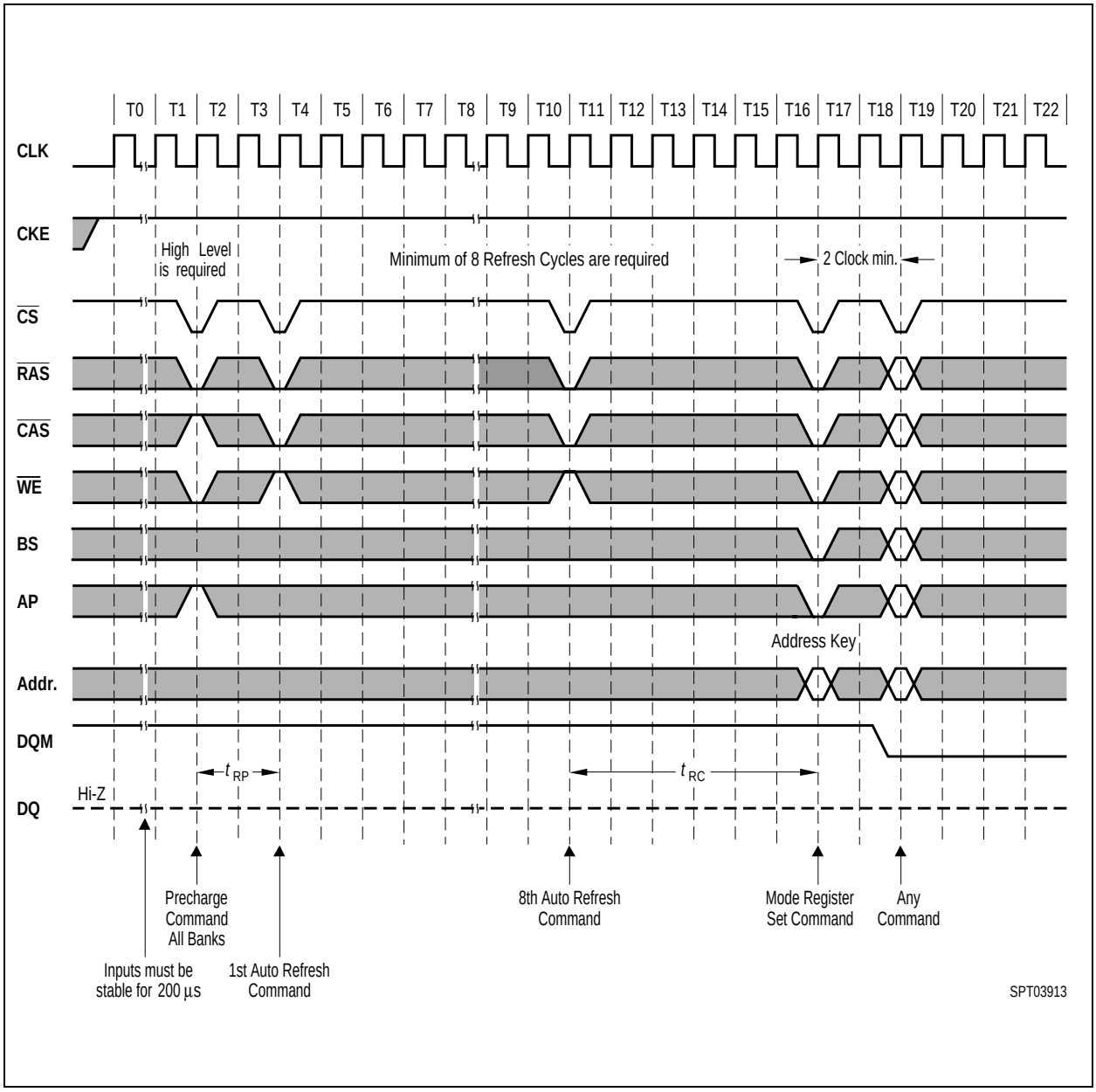
## 8.2 AC Parameters for a Read Timing



## 9. Mode Register Set

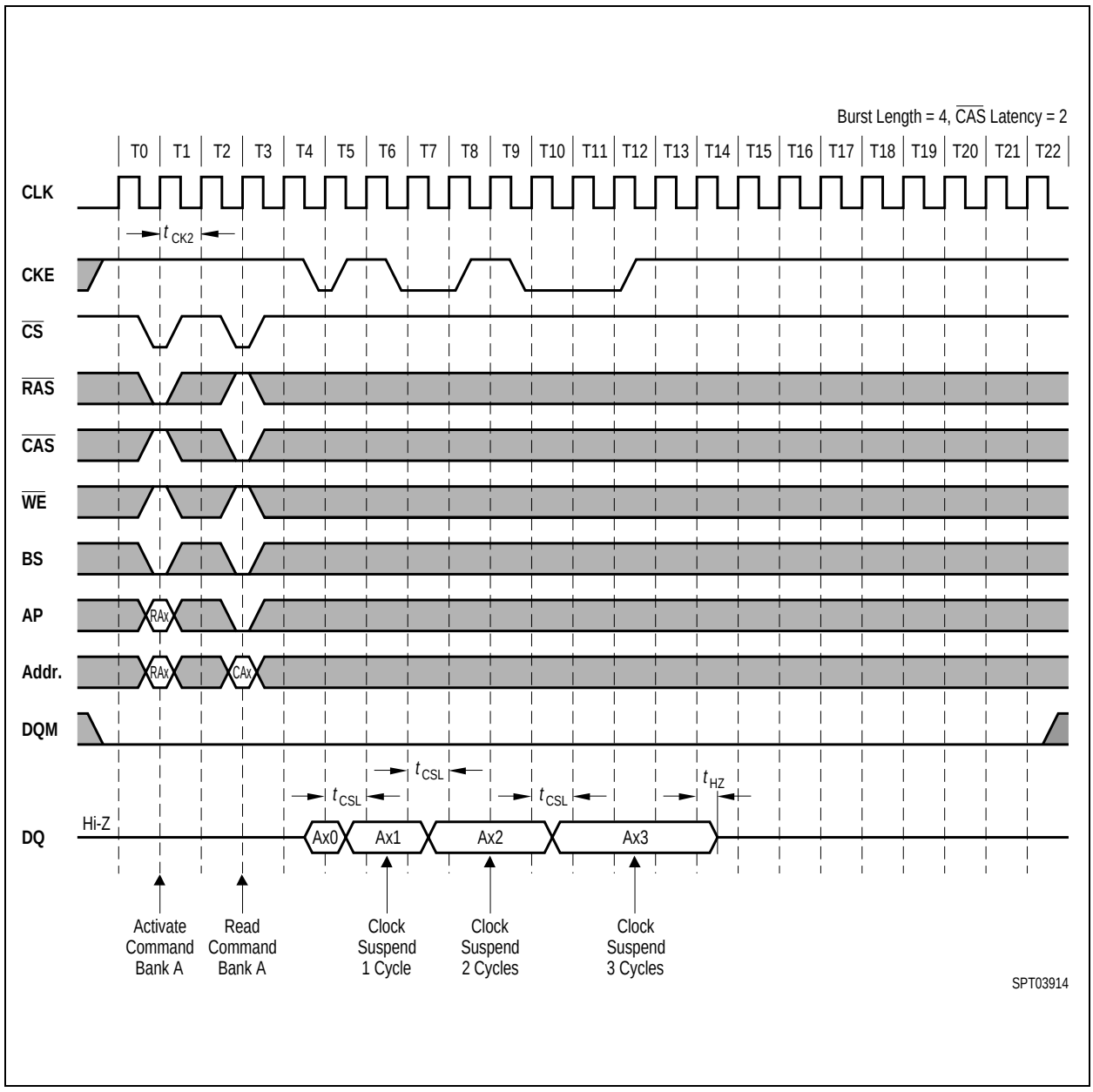


## 10. Power on Sequence and Auto Refresh (CBR)

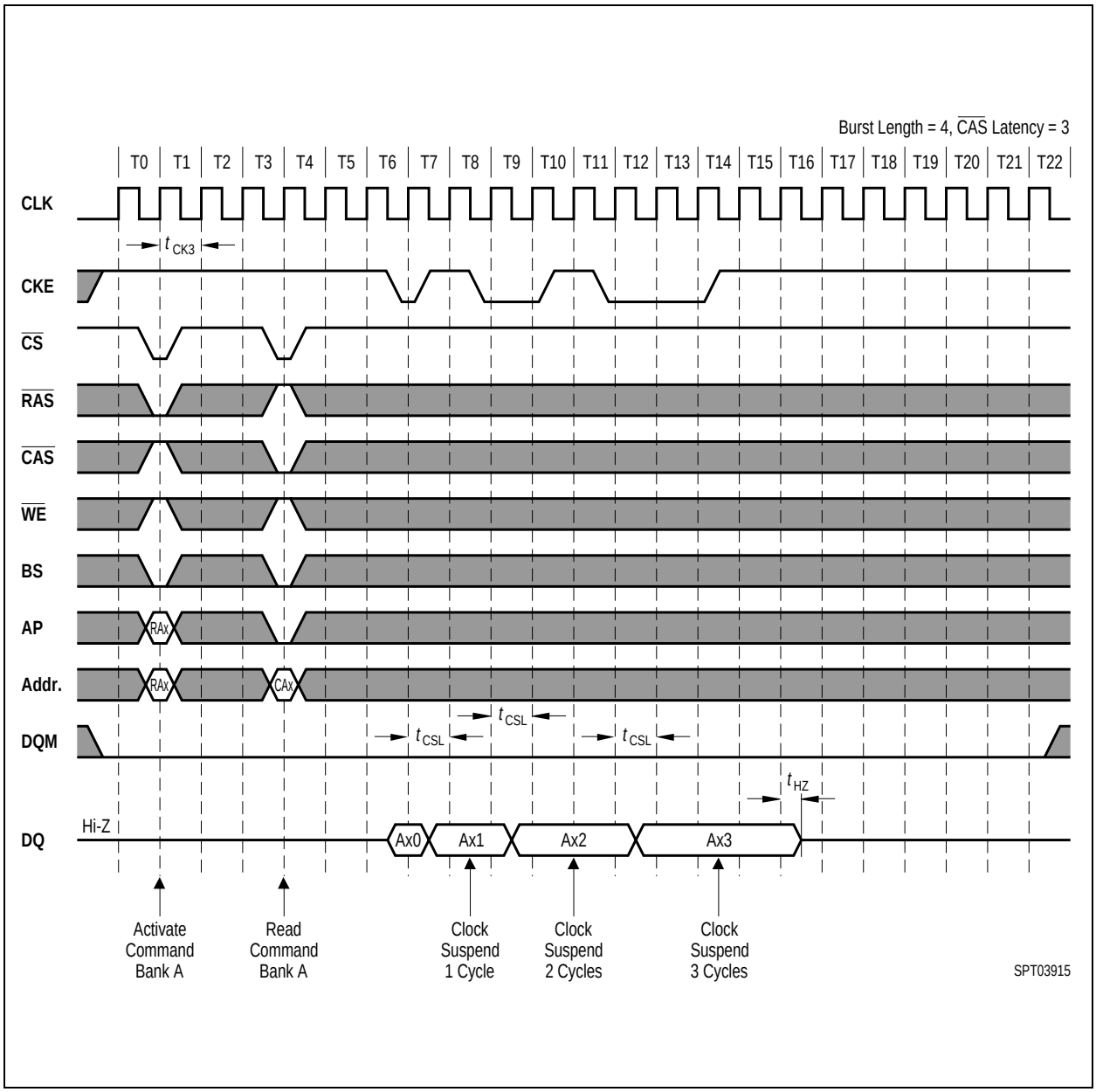


## 11. Clock Suspension ( Using CKE)

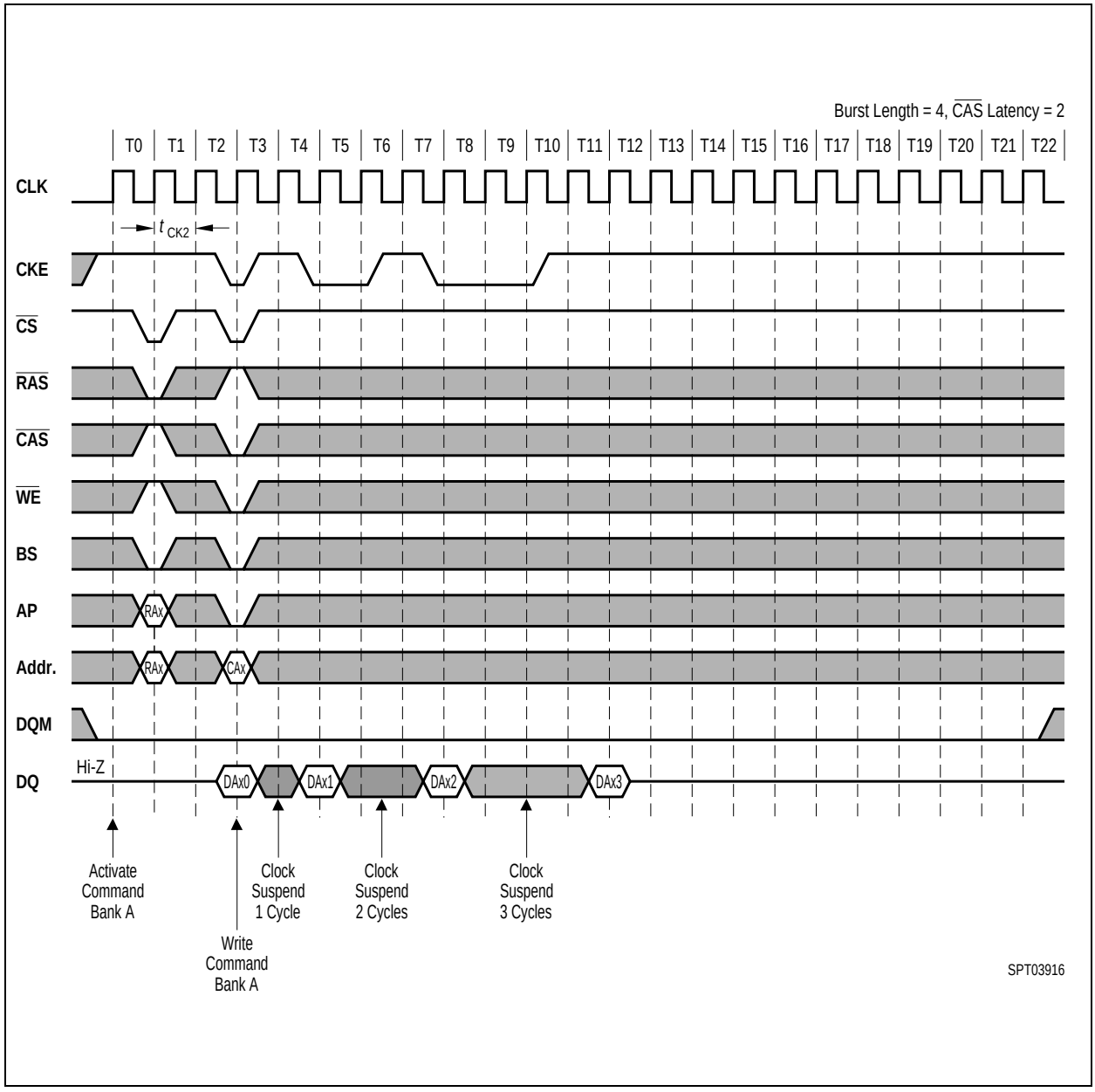
### 11.1 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 2



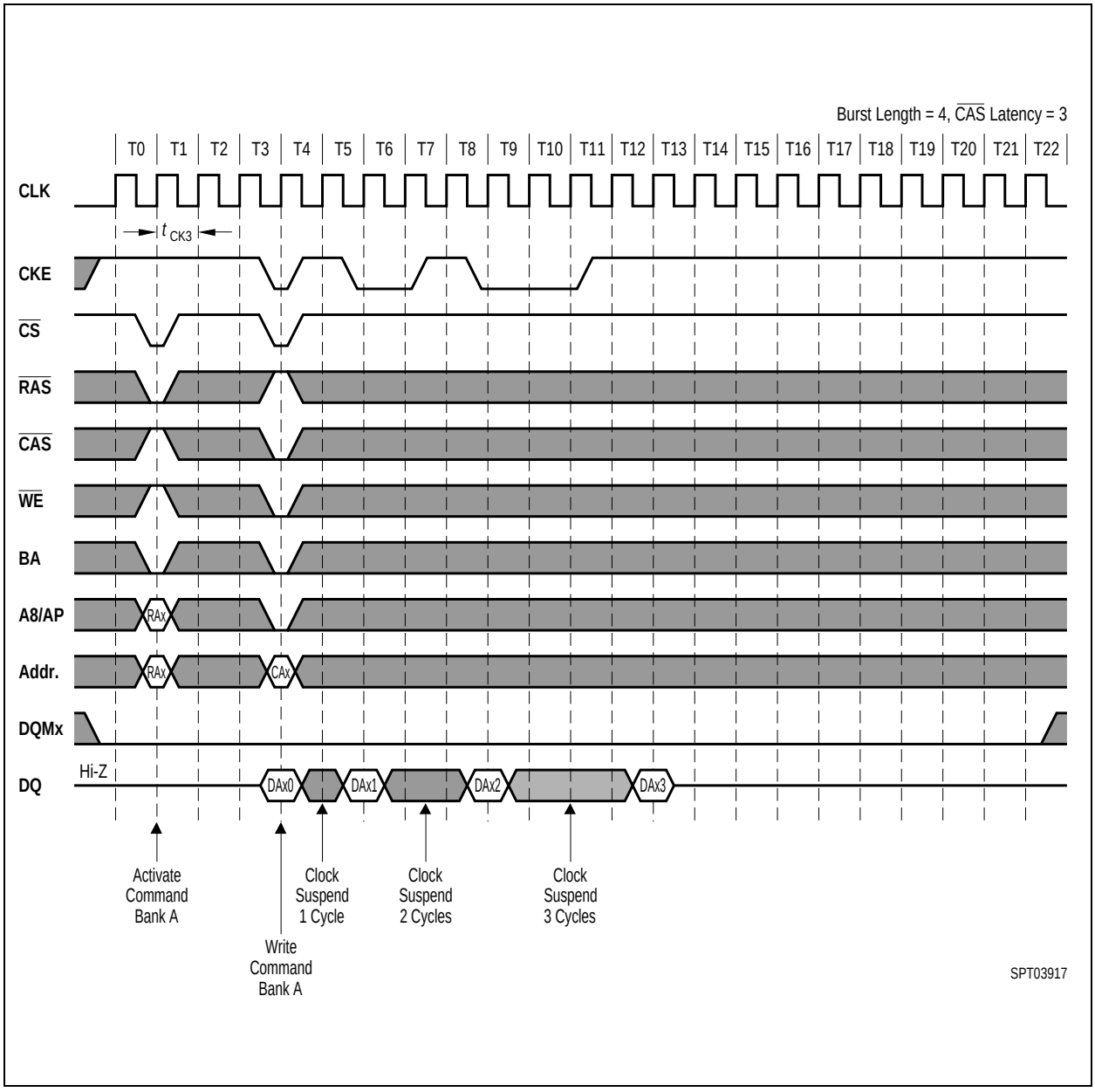
## 11.2 Clock Suspension During Burst Read $\overline{\text{CAS}}$ Latency = 3



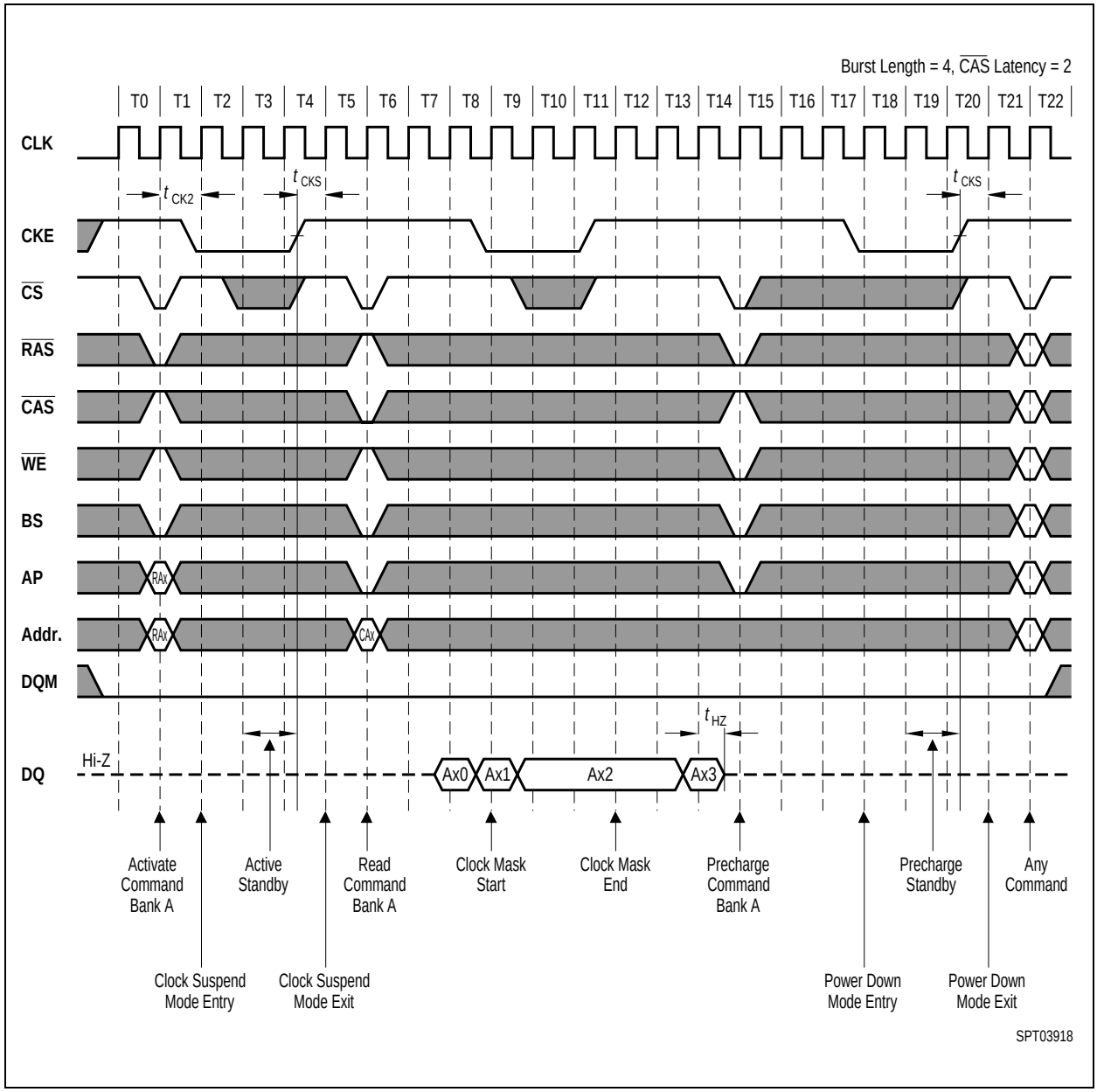
## 11.3 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 2



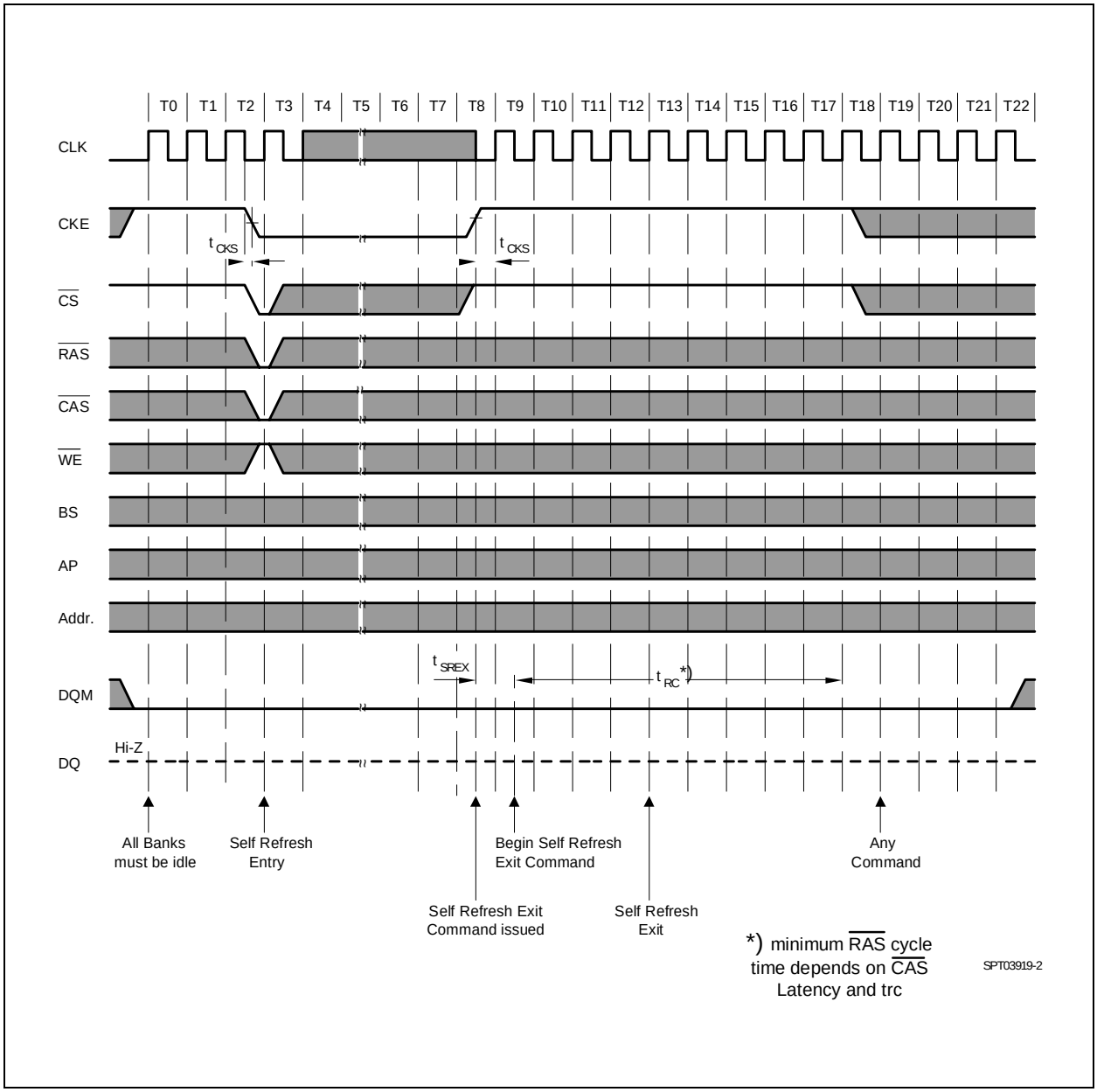
## 11.4 Clock Suspension During Burst Write $\overline{\text{CAS}}$ Latency = 3



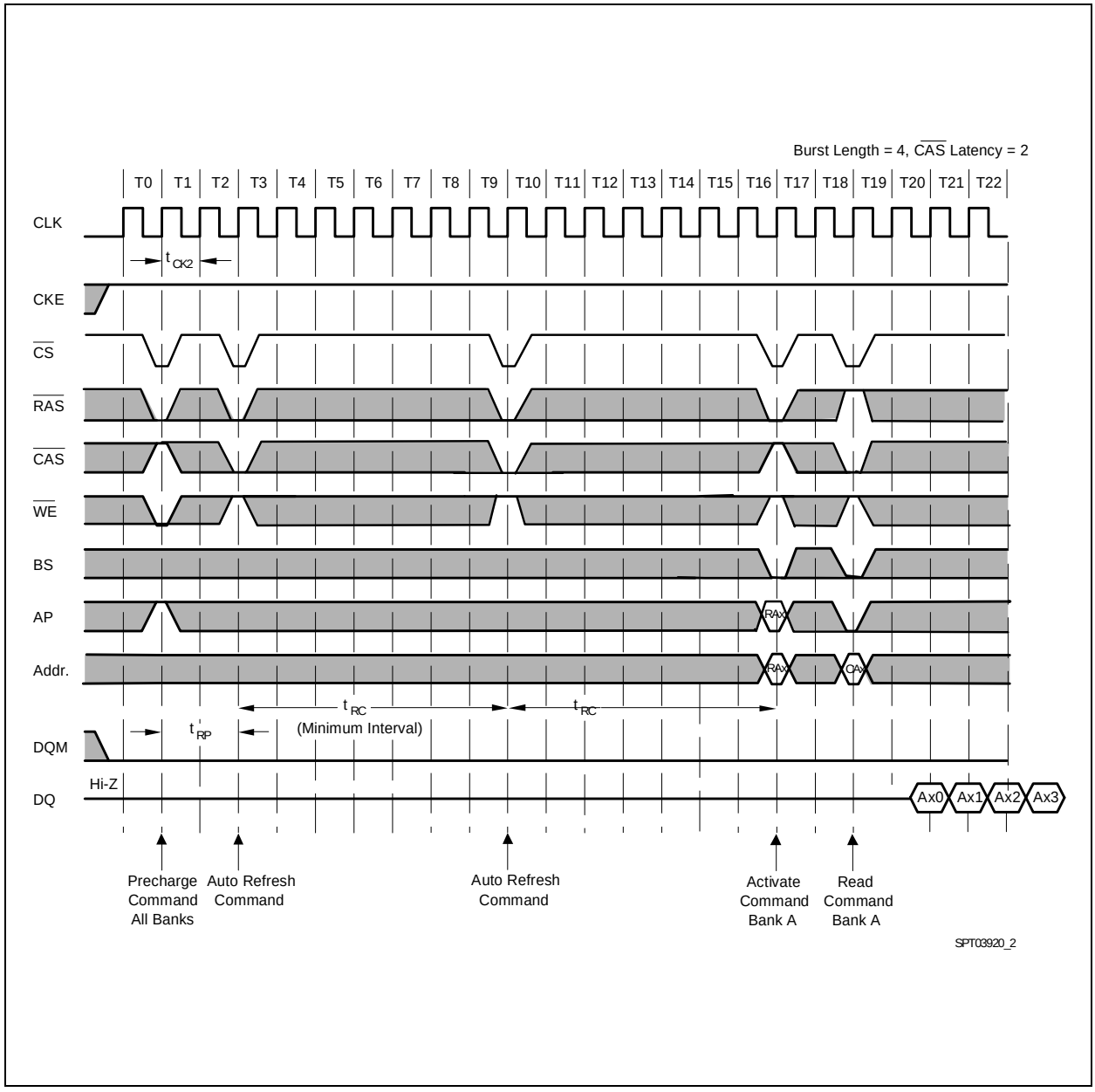
## 12. Power Down Mode and Clock Suspend



## 13. Self Refresh (Entry and Exit)

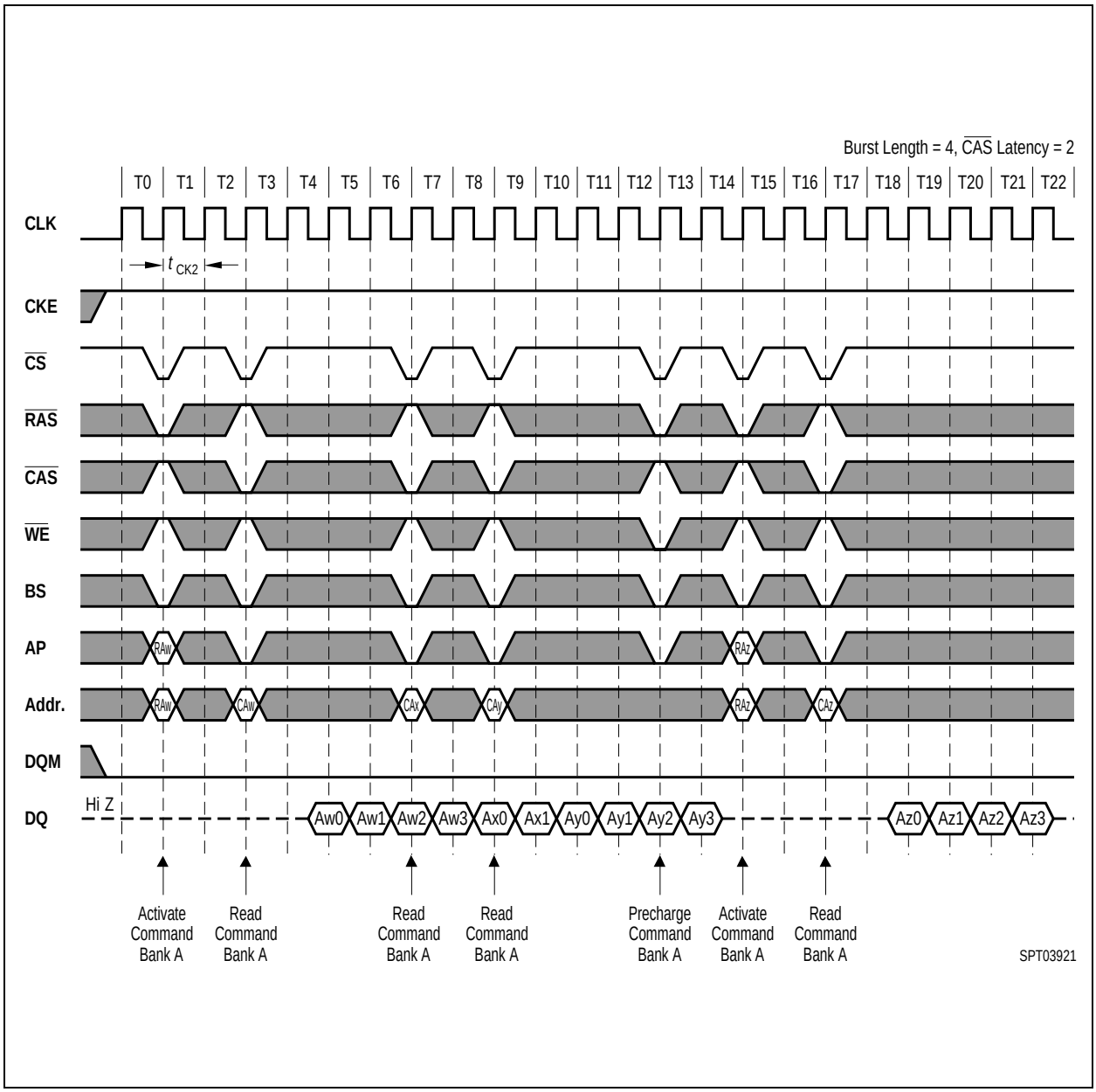


## 14. Auto Refresh (CBR)

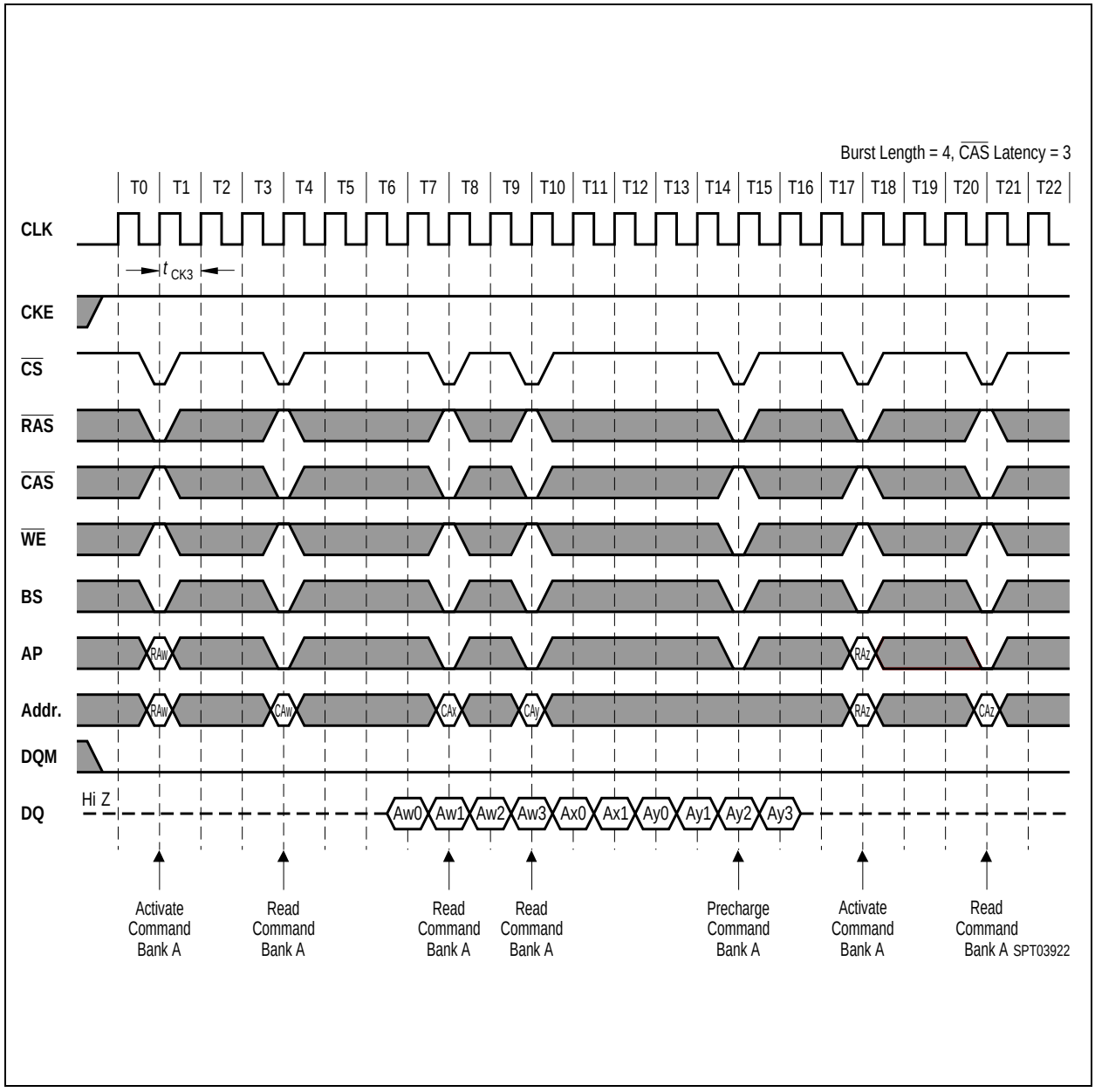


## 15. Random Column Read (Page within same Bank)

### 15.1 $\overline{\text{CAS}}$ Latency = 2

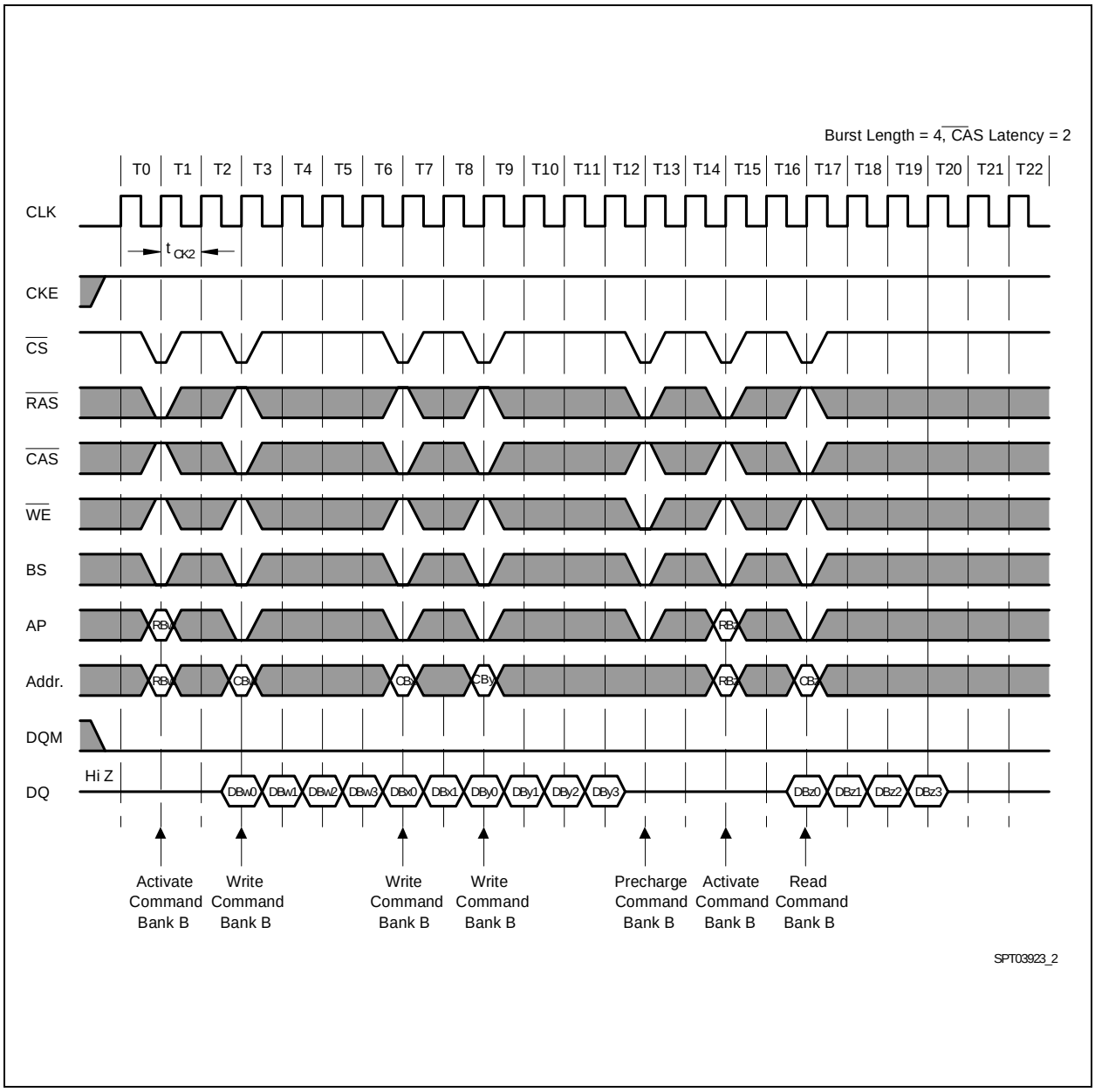


## 15.2 $\overline{\text{CAS}}$ Latency = 3

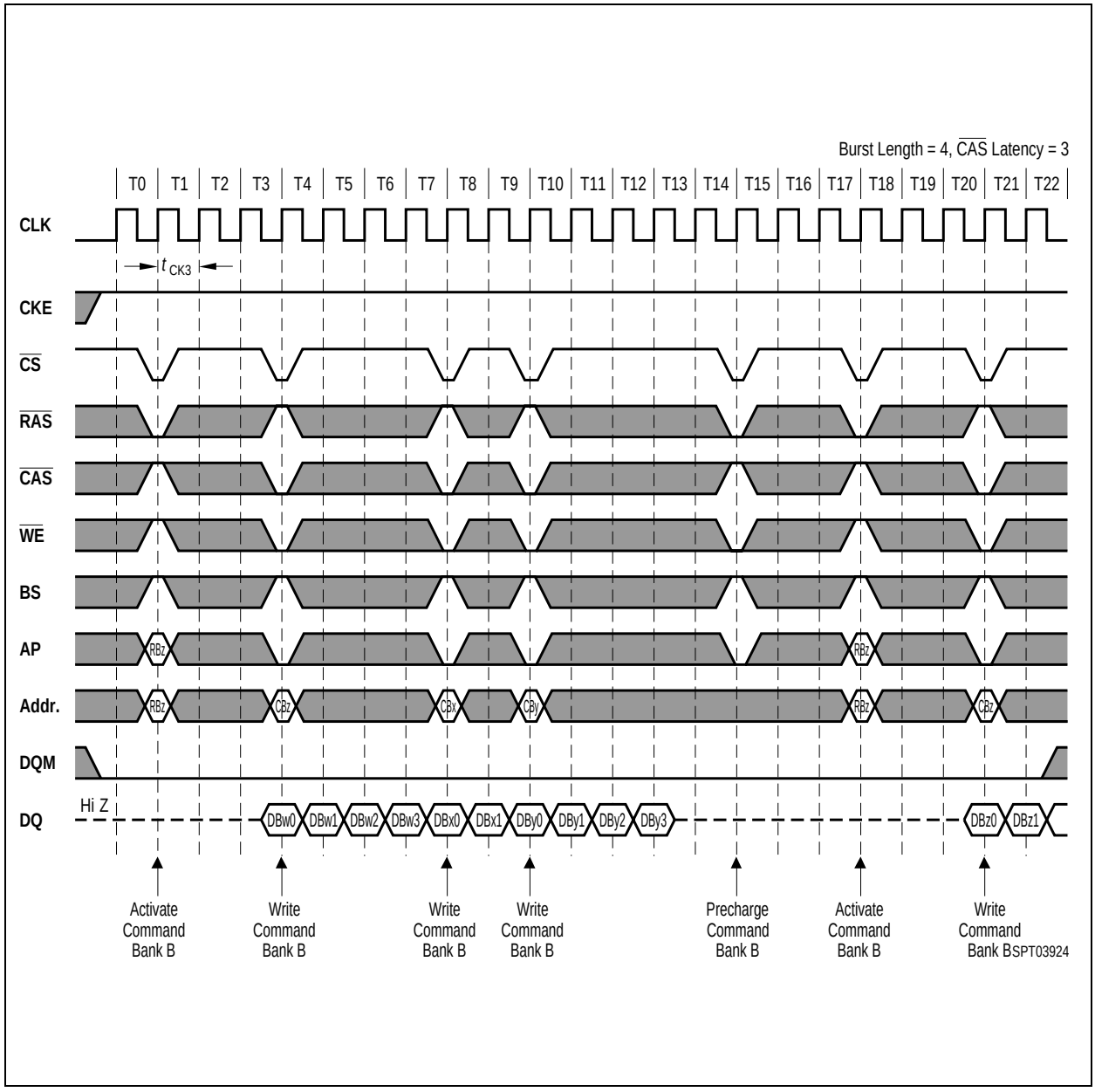


# 16. Random Column write (Page within same Bank)

## 16.1 $\overline{\text{CAS}}$ Latency = 2

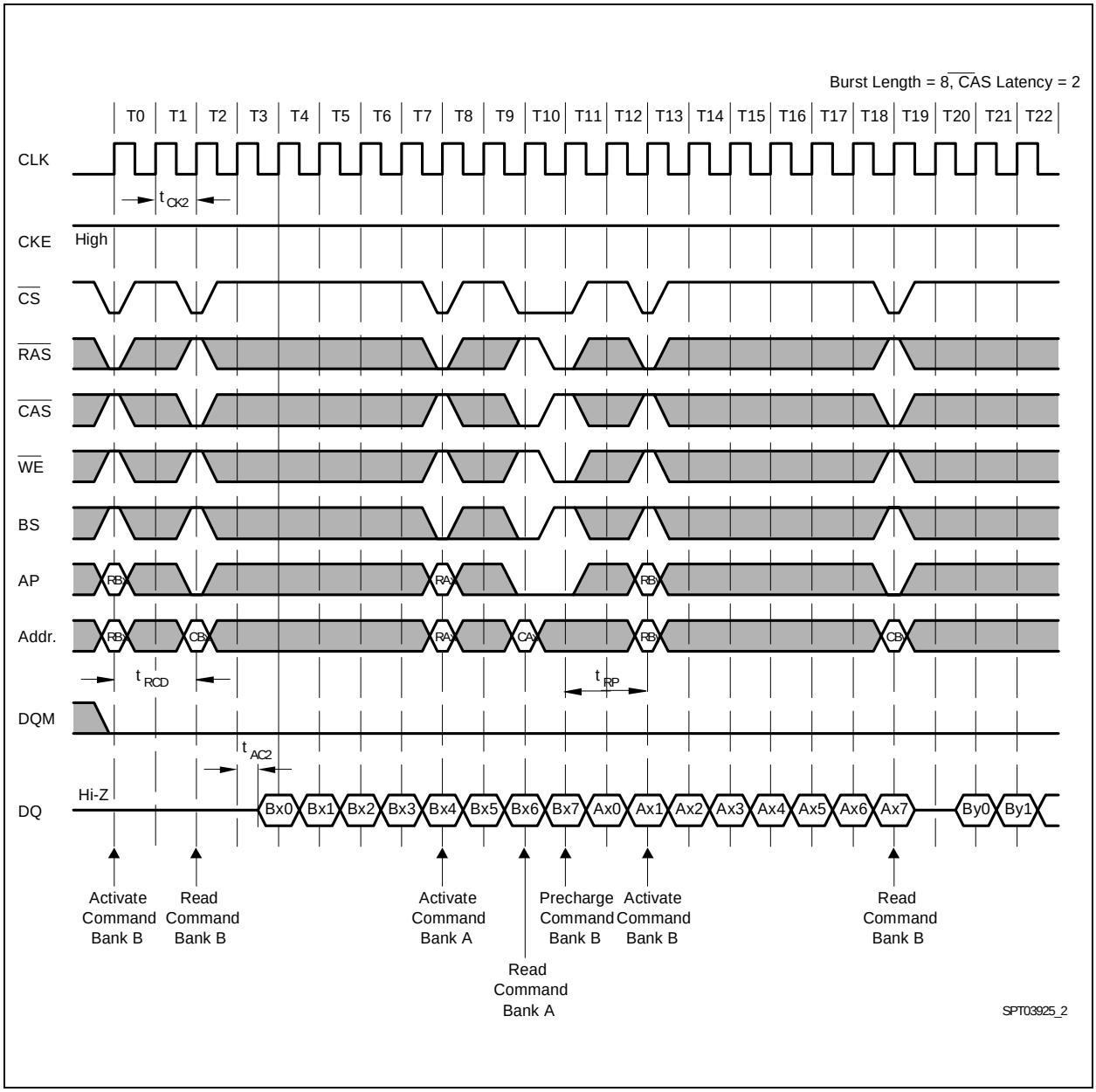


## 16.2. $\overline{\text{CAS}}$ Latency = 3

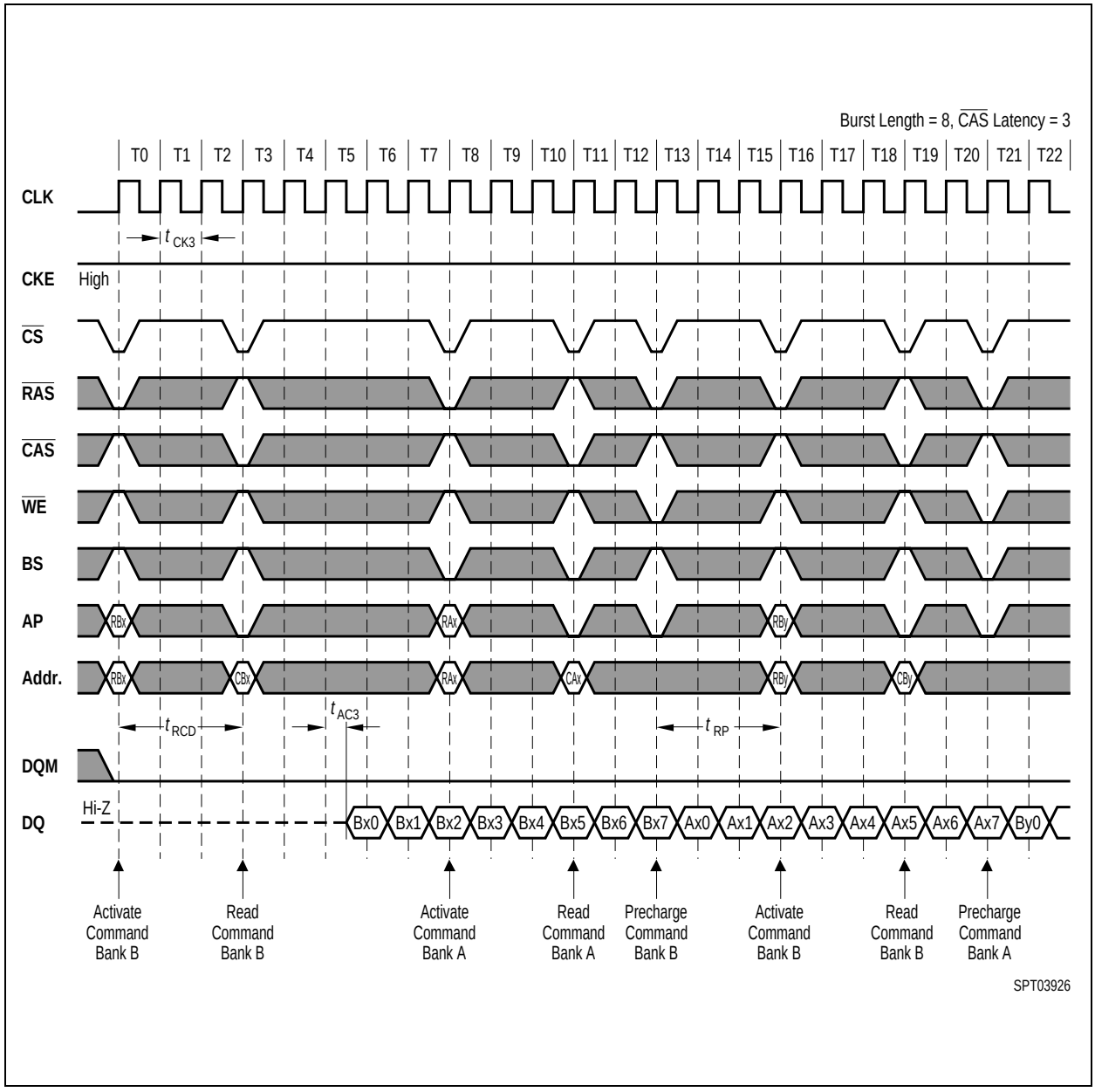


## 17. Random Row Read (Interleaving Banks) with Precharge

### 17.1 $\overline{\text{CAS}}$ Latency = 2

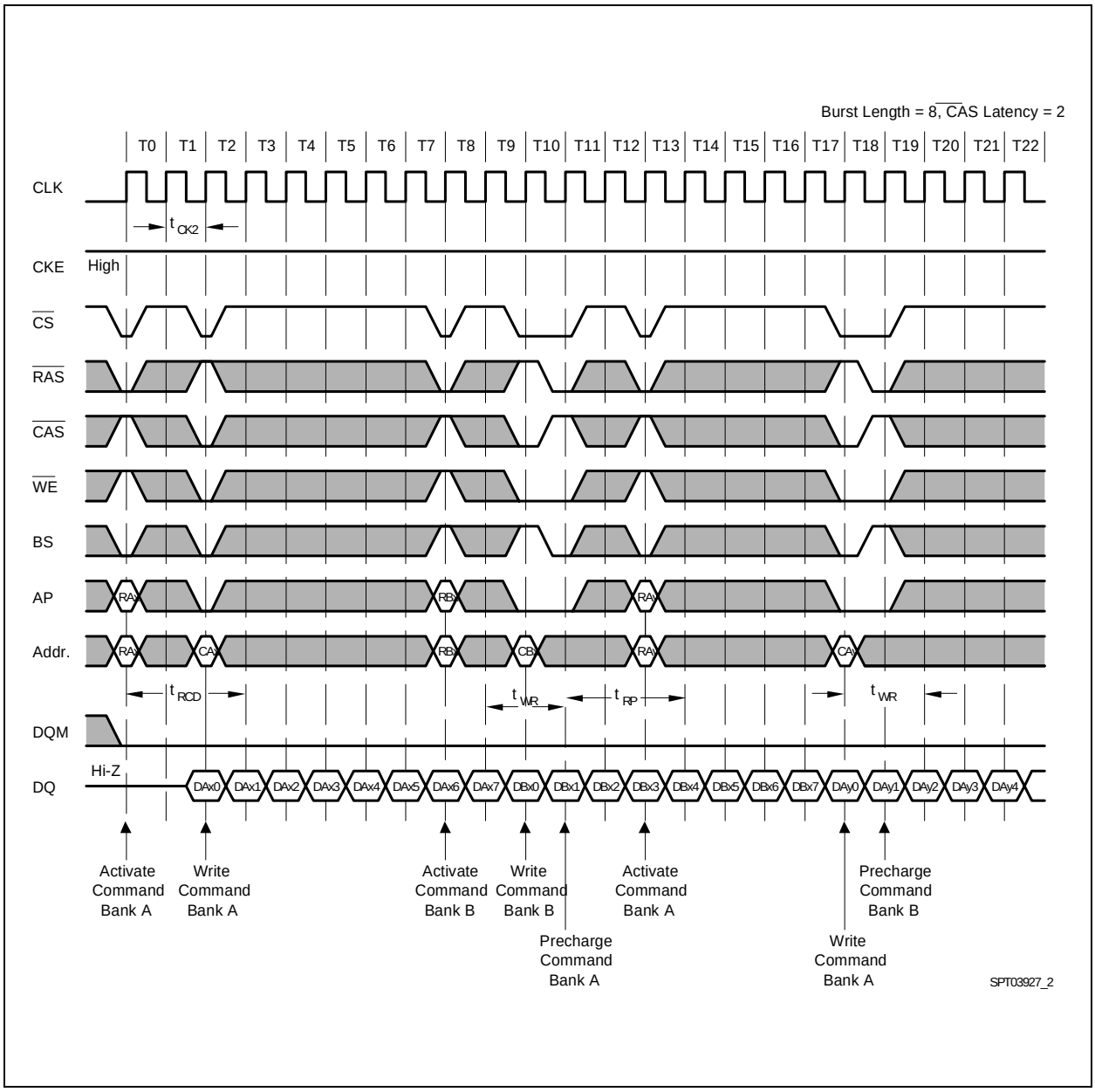


## 17.2 $\overline{\text{CAS}}$ Latency = 3

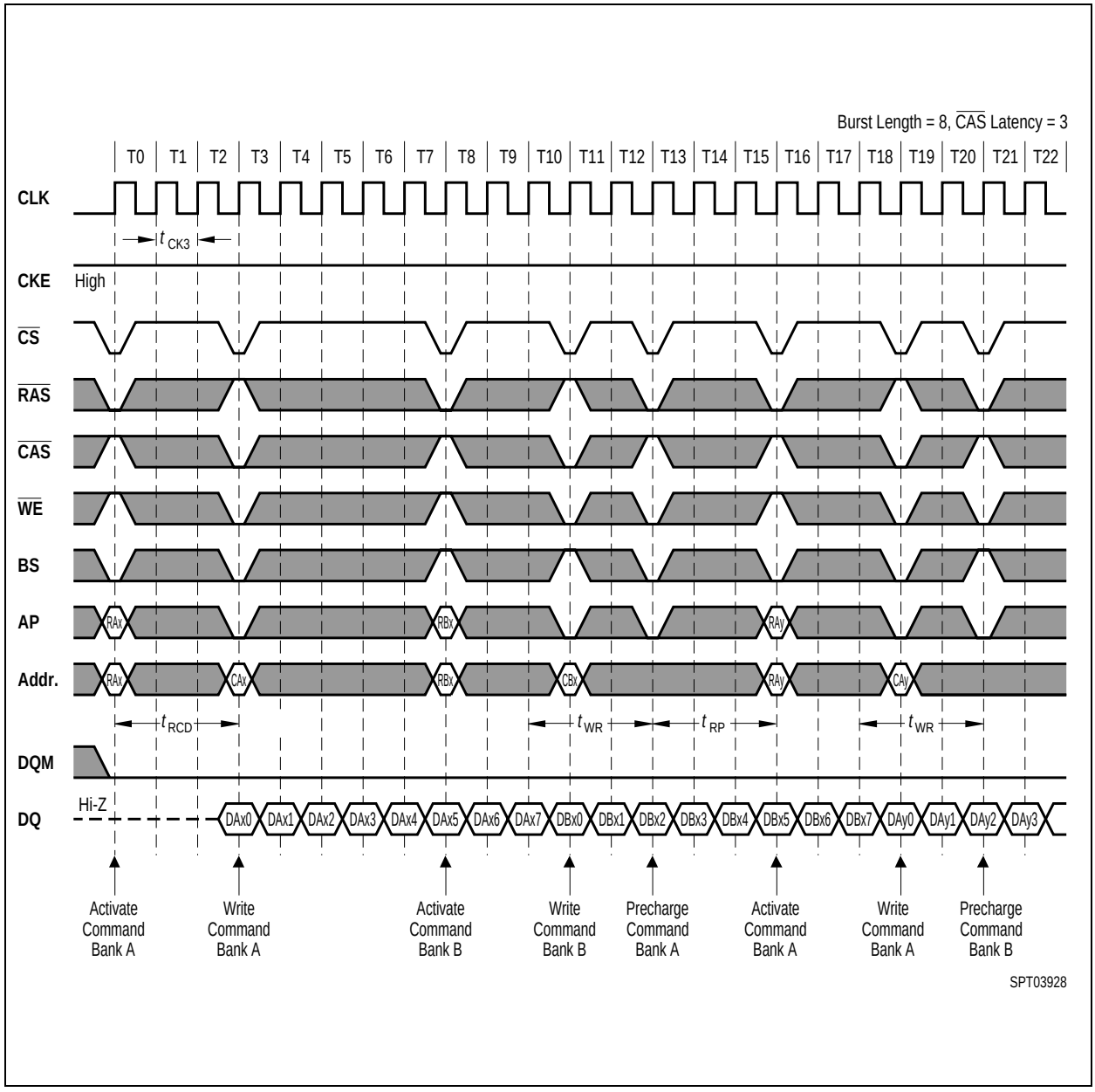


## 18. Random Row Write (Interleaving Banks) with Precharge

### 18.1 $\overline{\text{CAS}}$ Latency = 2

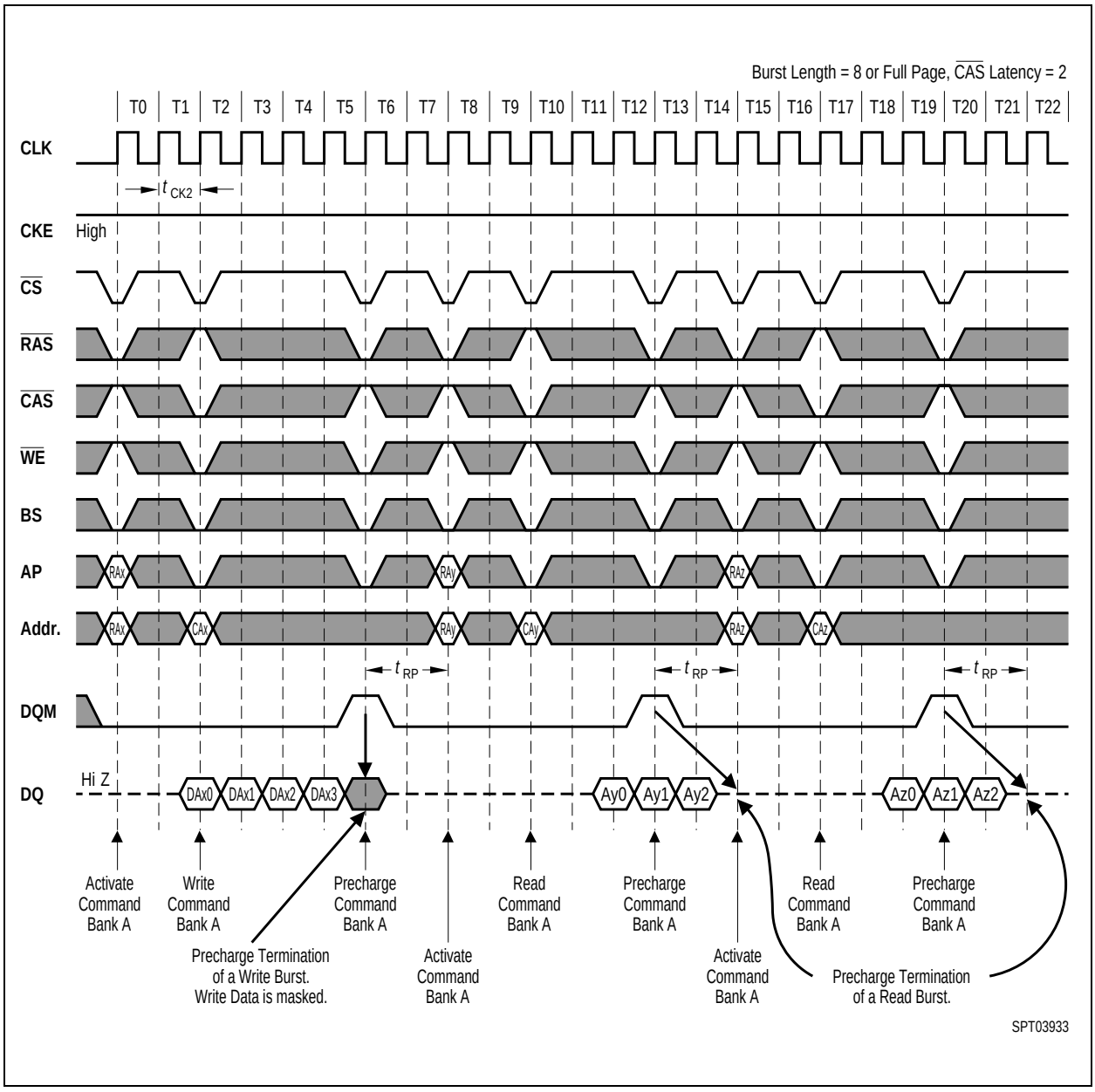


## 18.2 $\overline{\text{CAS}}$ Latency = 3



## 19. Precharge termination of a Burst

### 19.1 $\overline{\text{CAS}}$ Latency = 2



# Change List

| | |
|---|---|
| 23.8.99 | First Rev. |
| 6.10.99 | Clock Suspend Mode not supported anymore (Dr.Savignac)<br>Changes on pages 1, 8 & 15<br>Waveforms: chapters 11 & 12 deleted and renumbered |
| 3.12.99 | some PC133 parameters changed according to INTELs PC133 specification |
| 27.1.2000 | Some ICC currents changed after measurement of first lots<br>Datasheet changed from Target to Preliminary |
| 11.4.2000 | confusion note 4 on page 8, removed, burst stop is supported for BL =2,4 & 8 |
| 14.4.2000 | Full page burst is functional beginning with designstep DD3A.<br>Implemented into the datasheet as optional (untested) feature<br>Mail from Ralf Schneider, April 12. 00 |
| 25.4.2000 | Power Down Exit with one clock beginning with DD3D designstep<br>Clock suspend mode functional with DD3D designstep<br>Clock suspend mode is added in the datasheet and the waveform drawings again.<br>Tras interlock changed to 4 clocks<br>twr = 2 Clock on this design version<br>Note for availability of components with twr = 1 clock interlock |
| 28.6.2000 | Preliminary datasheet changed to final<br>Change request from Mr. Lüken:<br>Text change on page 16 (for clarification)<br>page 17: “mode register set-up time” renamed to “Mode Register set to Active delay”<br>Waveform Drawing changed from SPT03910 to SPT03910_2<br>Waveform Drawing changed from SPT03923 to SPT03923_2<br>Waveform Drawing changed from SPT03925 to SPT03925_2<br>Waveform Drawing changed from SPT03927 to SPT03927_2 |
| 20.7.2000 | Last minute changes requested by Mr. Lüken<br>page 16: note 4 for ICC1<br>Waveform Drawing changed from SPT03911 to SPT03911_2<br>Waveform Drawing SPT03925_2 trp arrow corrected |
| 8.8.2000 | ICC6 for Low Power Versions changed from 1.5 to 1.7 mA<br>(Discussion with Hahn and Lüken) |